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Nanoscale FinFET Based 6T SRAM Cell Design Analysis for Leakage Power Reduction

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ABSTRACT: At nanoscale technology nodes, various parameter variations and short channel effects greatly impact the semiconductor devices. The innovative and holistic circuit-level methodology is required to trade between power, area, and robustness while maintaining adequate manufacturing yield. FinFET based design as an alternative solution to the bulk devices for reducing short channel effects and leakage power. Many approaches have been earlier implemented to minimize the leakage power but were only able to minimize the fraction of leakage power. I have proposed a Hybrid technique and implemented it on a FinFET based 6T SRAM cell. It reduces the power dissipation in standby mode as leakage current is minimized and without charging the area penalty. Compared to the conventional FinFET, we achieved a reduction in leakage current and static power dissipation at 25.59% and 31.29% respectively at a constant 45nm channel length on Cadence virtuoso at room temperature.

KEYWORDS: SRAM, Leakage current, Leakage power, AVL, MTCMOS, Hybrid

1. INTRODUCTION

Rising demand for multimedia rich applications like portable and handheld devices have tremendously increased the need for large and high-performance memories like the Static Random-Access Memory (SRAM). The on-die cache memory occupies a large portion of the silicon area, i.e., of the total chip area. It also plays a significant role in overall power consumption of the multimedia application. Due to continuous scaling of the CMOS devices, it is possible to have a high packaging density which helps in reducing the overall Si area [1]. To minimize the overall power consumption, the first design factor loved by the designer community is the supply voltage (V_{DD}) reduction. This reduction in V_{DD}, though appreciates the power consumption, results in two important concerns, the data stability, and the leakage power. The leakage current composes nearly 40% of total power consumption in today's high-performance chip.

As MOSFETs are scaled down to the nanoscale regime, statistical dopant fluctuations, oxide thickness variations, and line-edge roughness increase the spread in transistor threshold voltage (V_{th}) and thus the on- and off- currents. In future technologies, Due to the reduction in threshold voltage, power consumption of memory devices is very high. So, the major problem concerned in the future SRAM cell is the power consumption. The FinFET transistor structure has been developed as an alternative to the bulk-Si MOSFET structure for improved scalability [2]. It utilizes a Si fin (rather than a planar Si surface) as the channel/body; the gate electrode straddles the fin. The fin width is the effective body thickness, and the fin height is the effective channel width. In the on state, current flows between the source and drain along the gated sidewall surfaces of the Si fin. Short-channel effects (SCE) are suppressed by utilizing a thin body, i.e., by making the fin very narrow, less than the channel length.

2. BACKGROUND AND REVIEW

Optimization of the device structure is extremely important for low-power and reliable SRAM cell design on 45 nm FinFET technologies. Robust FinFET based SRAM cell design at 45nm technology

should make sure minimum sensitivity to parameter variations along with proper functionality and low leakage power [2]. We also analyze static power and leakage current with variation of width of access, load, and driver FinFET transistor. All the analyses have been carried out for the static leakage power on the FinFET based SRAM cell on Cadence virtuoso simulation tool. Figure 1 shows the DG-FinFET device structure.

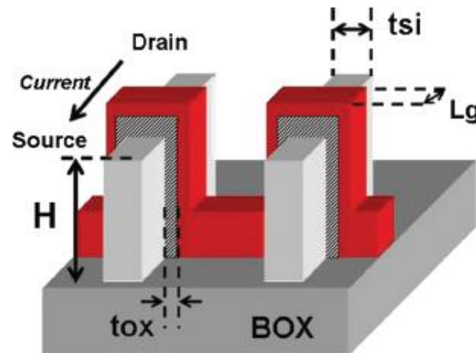

Figure 1. Double gate FinFET device structure.

The FinFET device is the most prominent candidate at sub 45 nm technology due to it is reducing various short channel effects and low parameter variability. FinFET is used to design various memory circuits on nanoscale level that require low power dissipation and acceptance to the environmental condition. In addition, FinFET based SRAM cells offer better switching speeds and superior noise margins as well. At a 45 nm node, Bulk MOSFET memory cell design is challenged by increased short channel effects (SCE) and sensitivity to parameter variations. We know that the size of a FinFET device affects the performance and the power dissipation of the memory circuit [3]. So, it is very difficult to design the optimized circuit. All the circuits are implemented with DG-FinFET based transistors with shorted gate terminals.

The 6T SRAM cell consists of two cross coupled inverters and two access FinFET transistors shown in Figure 2; these cross coupled inverters are called latch. The two cross coupled inverters have four transistors (M3, M4, M5, and M6); each bit in an SRAM is stored on these four FinFETs. Source terminals of both access FinFET (M1 and M2) are connected to the bit line (BL) and bit line bar (BLB). When the word line is low, access FinFET are OFF and bit lines are isolated from latch. In this state, the latch can hold the bit if the voltages remain at V_{DD} and V_{SS}. When the word line is high, access FinFET are ON, and bit lines (BL and BLB) are connected to the latch. The function of these bit lines is to transfer the data for both write and read operations [2]. SRAM cell operates in three modes of operation: Write mode: In this mode, SRAM cell can be written with a different bit value replacing its originally stored bit. Data retention or Hold mode: In this mode, the SRAM cell can hold the data for ever as long as it is powered. Read mode: In this mode, SRAM cell can communicate its stored data. This mode of operation does not affect the data. Table 1 shows the parameters used in the simulations in our SRAM cell design.

2.1 Write Operation

To perform the write operation, we must pull the word line high (WL="1") to activate the access transistors (M1 and M2). Now we can perform the write operation. The required data to be written is given to bit line (BL) and its complement is applied on bit line bar (BLB). This would make the cell to change its state accordingly. When state of latch is changed the word line is deactivated (WL="0") and thus the required data is written to the cell.

2.2 Hold operation

If the word line is not stated (WL=0), the access FinFET transistors (M1 and M2) disconnect SRAM cell from bit line (BL) and bit line bar (BLB). The two cross-coupled inverters formed by M3-M6 continue to reinforce each other as long as they are connected to the supply voltage (V_{DD}). The current flow in this state from the V_{DD} is called leakage current.

2.3 Read Operation

To read the data from the output node in the SRAM cell, the word line is first asserted to high (WL="1") which activates the access FinFETs (M1 and M2) to access the latch. Now both the bit lines (BL and BLB) are pre-charged to „1"and one of the bit lines would remain pre charged and the other would be discharged to ground, depending on the state of the latch. At this stage both the bit lines are applied at the inputs of the sense amplifier. This finally gives the information of the stored bit by amplifying the data to a significant level. Leakage current and static power dissipation waveform of FinFET based 6T SRAM is shown in Figure 3 and Figure 4 respectively.

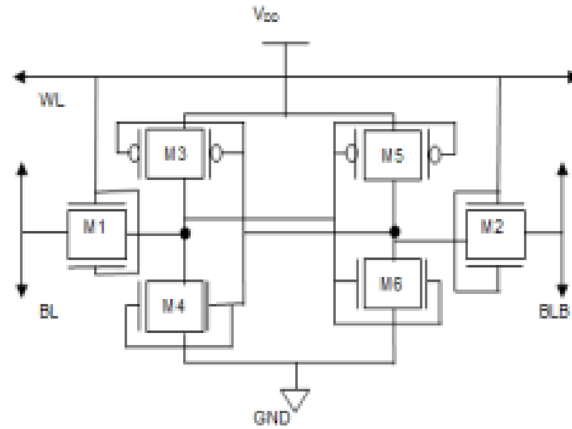

Figure 2. FinFET based 6T SRAM Cell.

Table 1. Parameter used in Simulation at 45nm node.

Parameters	Value
L_{eff}	45nm
T_{fin}	8.4nm
t_{ox}	1.5nm
H_{fin}	60nm
Channel doping	Intrinsic
Source/Drain Doping	$2\times10^{16}cm^{-3}$
$V_{to,n}$	0.31v
$V_{to,p}$	-0.25v
V_{DD}	0.7v

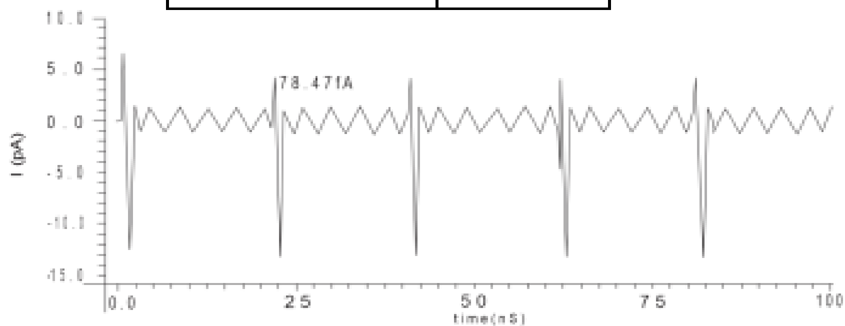

Figure 3. Leakage current of FinFET based 6T SRAM Cell.

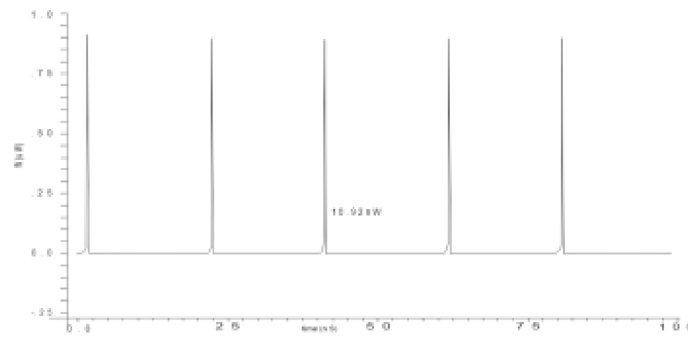

Figure 4. Static power dissipation of FinFET based 6T SRAM Cell.

3. PREVIOUS DESIGN TECHNIQUE FOR LEAKAGE POWER REDUCTION

a) AVL Technique

An Adaptive Voltage Level (AVL) which allows full supply voltage to be applied in active mode and reduced supply voltage in inactive mode appears to be particularly promising for reducing gate leakage currents as well [4].

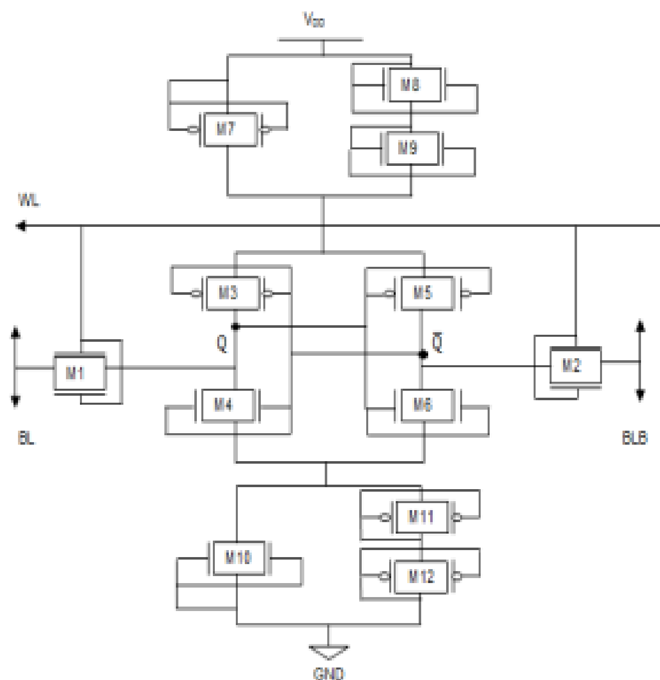

Figure 8. Implementation of AVL technique on FinFET based 6T SRAM cell.

A technique similar to the use of AVL for raising the ground potential has already been reported to yield significant reduction in gate leakage current [5,6]. So, in this work, in order to suppress the leakage further, the proposed SRAM cell combined with adaptive voltage level (AVL) circuit either at the ground node (referred as AVLG) or the supply node (referred as AVLS) is simulated, and its leakage characteristics are analyzed. Both of these circuits are termed as AVLG (lower AVL) and AVLS (upper AVL) respectively which together provide the reduced leakage to the FinFET based 6T SRAM cell. As shown in Figure 5, the circuit of FinFET based 6T SRAM cell by implementing the AVL technique. Leakage current and static power dissipation waveform of FinFET based 6T SRAM implemented using the AVL technique is shown in Figure 6 and Figure 7, respectively.

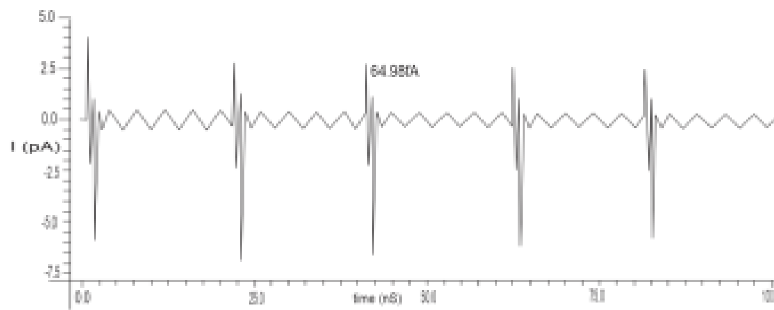

Figure 6. Leakage current waveform by applying AVL technique on FinFET based 6T SRAM Cell. SRAM.

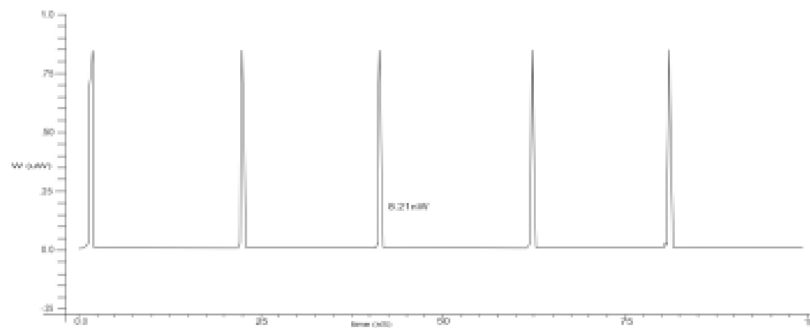

Figure 7. Static power dissipation by applying AVL technique on FinFET based 6T SRAM Cell.

b) MTCMOS Technique

Multi-threshold CMOS is a variation of CMOS chip technology which has transistors with multiple threshold voltages (V_{th}) in order to optimize delay or power. The V_{th} of a MOSFET is the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. Low V_{th} devices switch faster and are therefore useful on critical delay paths to minimize clock periods. The penalty is that low V_{th} devices have substantially higher static leakage power. High V_{th} devices are used on non-critical paths to reduce static leakage power without incurring a delay penalty. Typical high V_{th} devices reduce static leakage by 10 times compared with low V_{th} devices [7].

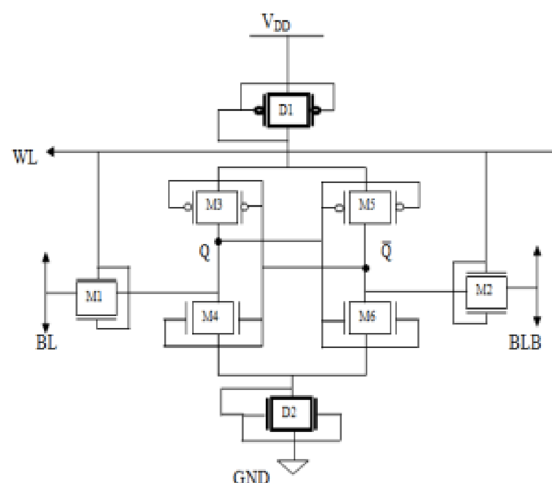

Figure 8. Implementation of MTCMOS technique on FinFET based 6T SRAM cell.

In MTCMOS technique, transistors of low threshold voltage become disconnected from power supply by using high threshold sleep transistor on the top and bottom of the logic circuit. Transistor having low threshold voltage (low-V_{th}) is used to design logic as shown in Figure 8. The sleep transistors are controlled by the sleep signal. During the active mode, the sleep signal is deserted, causing both high V_{th} transistors to turn on and provide a virtual power and ground to the low V_{th} logic. When the circuit

is in in-active mode, the sleep signal is asserted, forcing both high V_{th} transistors to cut-off and disconnect power lines from the low V_{th} logic. This results in a very low leakage current from power to ground in standby mode [8]. Leakage current and Leakage power waveform of FinFET based 6T SRAM implemented using the MTCMOS technique is shown in Figure 9 and Figure 10 respectively.

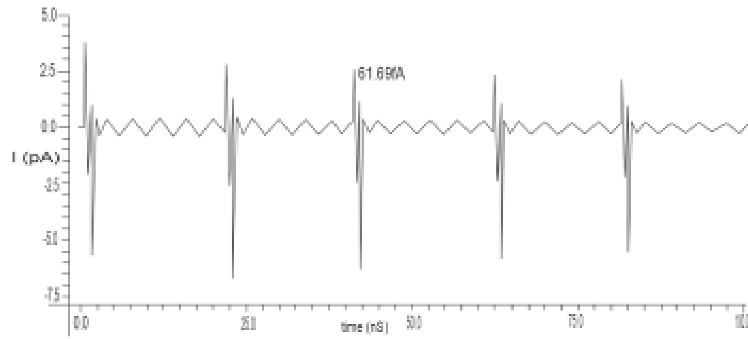

Figure 9. Leakage current waveform by applying MTCMOS technique on FinFET based 6T SRAM Cell.

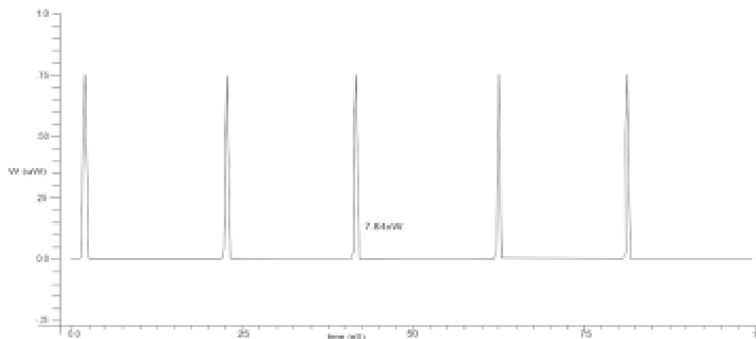

Figure 10. Static power dissipation by applying MTCMOS technique on FinFET based 6T SRAM cell.

4. PROPOSED HYBRID TECHNIQUE FOR LEAKAGE POWER REDUCTION

In Hybrid SRAM cell technique, a high threshold transistor is used which reduces the sub threshold leakage in the SRAM cell [9]. In active mode, the High V_{th} transistor must be ON to provide the usual circuit functionality of the 6T SRAM cell. In standby mode, the High V_{th} transistor must be OFF to provide better leakage control. However, the threshold voltage of all transistors may be changed. Though, it can increase the read delay of the SRAM cell. So, the threshold voltage of PMOS transistors is increased. Similarly, gate leakage is reduced by increasing oxide thickness of the NMOS transistor and pass transistor.

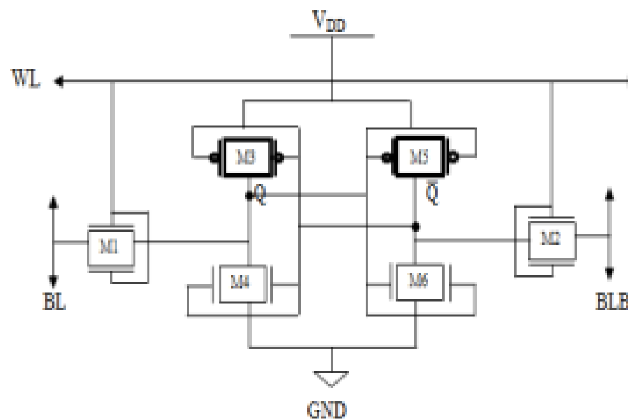

Figure 11. Implementation of Hybrid technique on FinFET based 6T SRAM Cell.

As shown in Figure 11, the circuit of FinFET based 6T SRAM cell by implementing the Hybrid technique. Output Waveform of Leakage current and static power dissipation for FinFET based 6T

SRAM cells implemented using the hybrid technique is shown in Figure 12 and Figure 13 respectively.

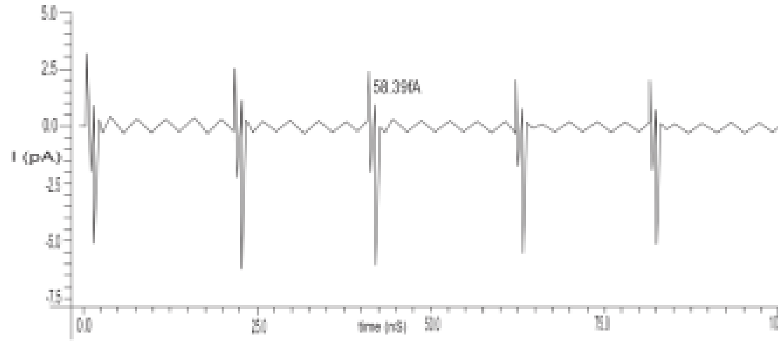

Figure 12. Leakage current waveform by applying Hybrid technique on FinFET based 6T SRAM cell

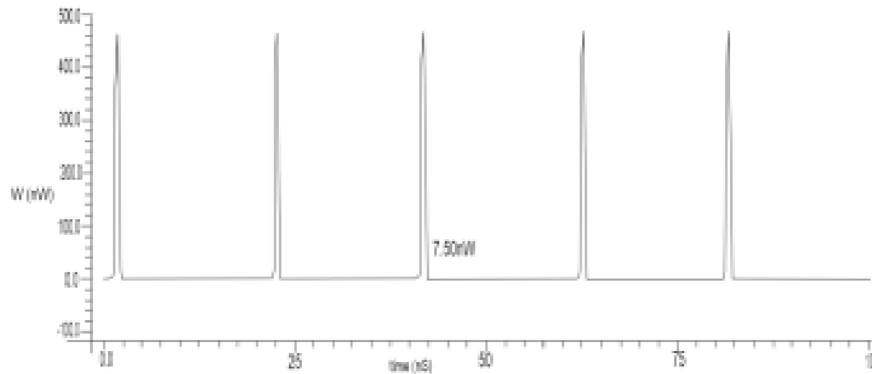

Figure 13. Static power dissipation by applying Hybrid technique on FinFET based 6T SRAM Cell.

5. RESULTS

Reducing the leakage aspects of the SRAM has been very essential to enhance the stability of the cell. The AVL technique reduces the leakage current and power dissipation by 17.19% and 24.81%. The MTCMOS technique reduces the leakage current and power dissipation by 21.38% and 28.17%. The proposed Hybrid technique reduces the leakage current and leakage power by 25.59% and 31.29%. Table II shows the Total leakage current and Leakage power for various SRAM topologies.

Table 2. Total Leakage Current & Leakage Power Analysis for Various Leakage Reduction Techniques

SRAM Topologies	Total Leakage Current	Leakage Power
6T FinFET	78.47×10^{-15}A	10.922×10^{-9}W
6T FinFET AVL	64.98×10^{-15} A	8.212×10^{-9} W
6T FinFET MTCMOS	61.69×10^{-15} A	7.843×10^{-9} W
6T FinFET HYBRID	58.39×10^{-15} A	7.504×10^{-9} W

6. CONCLUSION

In this paper, a novel leakage reduction technique is presented that reduces the sub threshold current and improves performance as compared with FinFET based 6T SRAM cells. Proposed SRAM cell has high threshold PMOS and high t_{ox} NMOS transistors in the critical path, whereas conventional design and other design based 6T SRAM cell containing the logic circuits are implemented in the noncritical path. Simulation results in a 45-nm industrial FinFET technology based proposed design technique highly reduces the leakage current and leakage power by 25.59% and 31.29%, without increasing the path delay over the FinFET based SRAM cell.

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