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Comparative Performance of CMOS Active Inductor

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Abstract. In this work, a Gyrator-C based CMOS active inductor is designed using 180nm and 90nm CMOS technology. Moving from 180nm to 90nm technology will diminish the cost of the system and provide more functionalities. The nominated circuit is designed using a three-stage Common Source (CS) configuration, and the resemblance is made with the recent work. From the simulation results, it is monitored that the maximum quality factor (Q_{max}) lifts, and the area sinks as we wane the technology. The consequences depict the Q_{max} of 311 at 478.63MHz and an area of 216.04μm^2 for 180nm technology. Whereas, the ensue for 90nm technology gives the Q_{max} of 659 at 10.96GHz and an area of 68.73 μm^2.

Keywords: Active Inductor (AI), Area, CMOS, Gyrator – C, Quality Factor (Q).

1 Introduction

Inductors are the heart of wireless communication and RF integrated systems [1], [2]. It plays an integral role in designing of Voltage Control Oscillator (VCO), Low Noise Amplifier (LNA), Impedance matching and gain boosting in wireless transceivers, bandwidth improvement in broadband data communication over the wire and optical channels. Generally, passive inductors are off-chip discrete components. However, the off-chip inductors have convinced obstructions of providing the limited bandwidth, reduce the reliability, and increase the outlay of the system by consuming more silicon area [3]. In the meantime, the need for a large silicon area to fabricate spiral inductors has also provoked great interest in and intensive research on the synthesis of inductors using active devices. The indispensable recognitions of CMOS Active Inductors (AIs) are less silicon area consumption, high-quality factor, large and tunable inductance value. The most fundamental capability of AIs is compact and broad tuning range [3]. Out of all this, there are few stumbling blocks of AI: poor linearity, higher noise, and less stability. [5], [6]. CMOS AIs is comprehended using varied methodologies in the industry. Mainly, there are two methods to realize the AI

circuits: op-amp based realization deals with MHz frequency, whereas; gyrator-C based realization deals with GHz frequency. Quality factor and size are compelling parameters. Common gate (CG) - common source (CS) gyrator-C based AI is discussed in Ref. [4]. Less number of transistors results in the small chip area and low power consumption of the AI circuit, but the higher value of parasitic series resistance and lower value of parallel resistance provide the lower value of the quality factor [6].

Nowadays, the challenging task is to shrink the channel length of CMOS active components. In the proposed work, 180nm and 90nm Conventional AI circuits are considered as shown in Fig.1. The proposed work shows the analogy of AI in 180nm and 90nm Technology. The quality factor upsurge as we reduce the CMOS technology in the frequency range of 10MHz to 100GHz. The peak quality factor for granted work is 311 at 478.63MHz for 180nm and 659 at 10.96GHz for 90nm. Moreover, the area for 180nm layout is 216.04 μm^2 whereas, for 90nm layout is 68.73 μm^2.

Fig. 1.

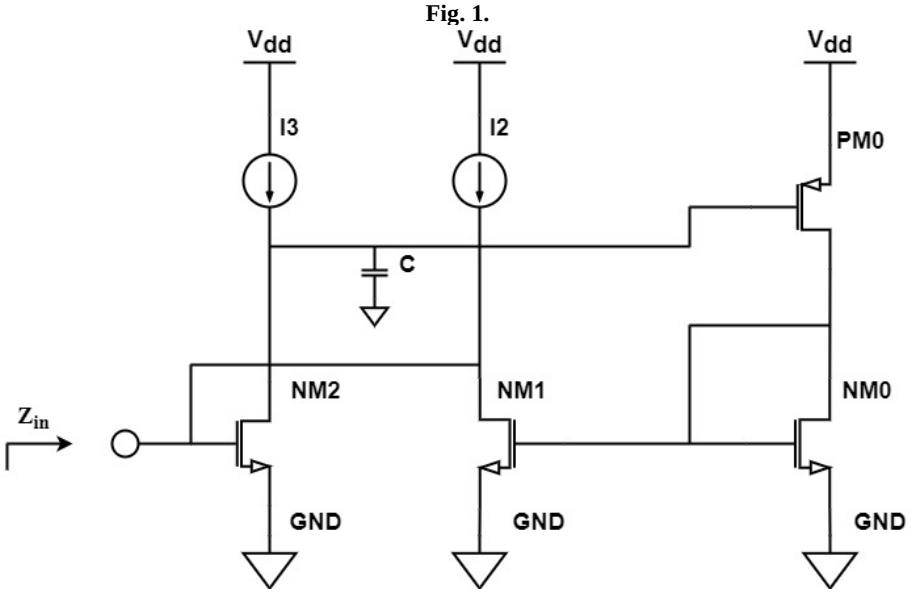

Fig. 1. Conventional Active Inductor Circuit

Two peculiar technologies are being implemented in the paper. In the first one, the AI circuit is being implemented by 180nm technology and the second same AI circuit is being implemented by 90nm technology. Both the technologies are being compared based on inductance value (L), Quality factor (Q), power dissipation (P_{diss}), silicon area, Monte Carlo analysis and PVT analysis.

2 Small Signal Model

The simplified small-signal model of Fig.1 is shown in Fig.2.

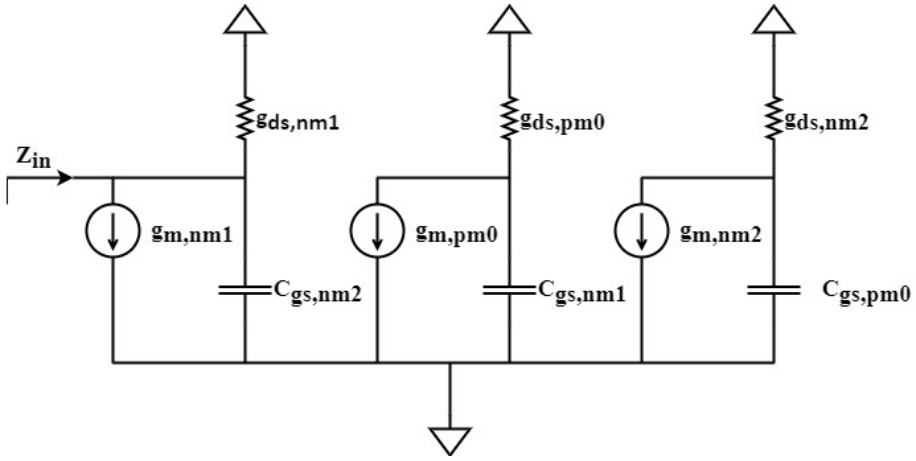

Fig. 2. Small Signal Model

RF Integrated circuit is being realized using the small signal model in order to know which parameters will affect which component during the simulation in high frequency. The inductance behavior can be seen in the frequency range where the phase is between +90º to −90º. Gyrator-C topology is being shown in Fig. Three and its equivalent passive model is shown in Fig. 4. During the inductor behavior, all the NMOS and PMOS are working in the saturation region. For small-signal model analysis, one assumption is being taken, and that is gate-source capacitance (C_{gs}) is much higher than the gate-drain capacitance (C_{gd}). The equation gives the input impedance Zin at the input port:

$$Z_{in} = \frac{1}{sC_{gs,nm2}} + \frac{1}{g_{ds,nm1}} + \frac{\left(sC_{gs,nm1} + g_{ds,pm0}\right)\left(sC_{gs,pm0} + g_{ds,nm2}\right)}{g_{m,nm1}g_{m,nm2}g_{m,pm0}} \tag{1}$$

$$Z'_{in} = \frac{sC_{gs,nm1} + g_{ds,pm0}\left(sC_{gs,pm0} + g_{ds,nm2}\right)}{g_{m,nm1}g_{m,nm2}g_{m,pm0}} \tag{2}$$

Now, by considering the values $C_{gs,\ nm1} <<< C_{gs,\ pm0} + C_{gs,\ nm2}$ the other components value can be derived as:

$$L_{eq} = \frac{C_{gs,pm0}\left(g_{m,pm0} + g_{m,nm2}\right)}{g_{m,nm1}g_{m,nm2}g_{m,pm0}} \tag{3}$$

$$R_s = \frac{g_{ds,nm2}\left(g_{m,pm0} + g_{m,nm2}\right)}{g_{m,nm1} g_{m,nm2} g_{m,pm0}} \tag{4}$$

$$C_d = \frac{1}{C_{gs,nm2}} \tag{5}$$

$$R_p = \frac{1}{g_{ds,nm1}} \tag{6}$$

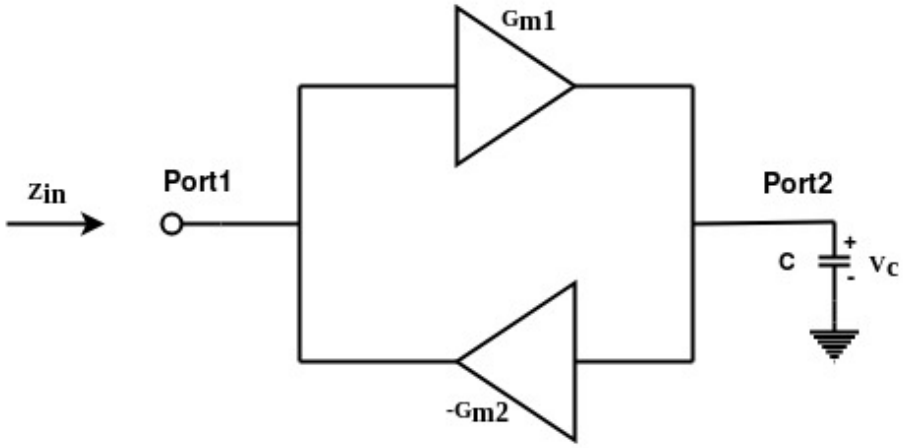

Fig. 3. Gyrator-C realization of Active Inductor [10]

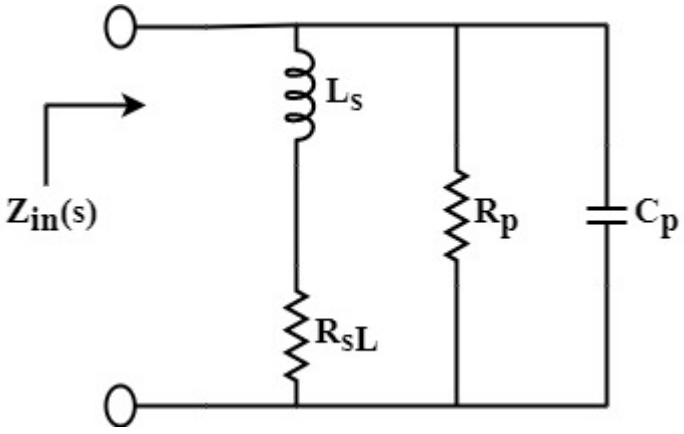

Fig. 4. Equivalent Passive Model [10]

Where, L_{eq}, R_s, C_d, R_p are equivalent inductors, series resistance, drain capacitance and parallel resistance of the AI circuit. Now from the above equation (3), we can see that the $C_{gs,\ pm0}$ can drive L_{eq}, and so the L_{eq} value increases. Moreover, the

scale of the transistor and its parasitic capacitance are connected [16]. The parasitic capacitance therefore increases with increasing the transistor size (W/L) [17]. Hence the inductance (L_{eq}) increases so the quality factor also gets enhanced.

The quality factor is driven by the Leq and equation is as below:

$$Q = \frac{wL_{eq}}{R_s} \tag{7}$$

The quality factor is one of the essential factors when we deal with applications like Current Control Oscillator (CCO) and bandpass filter. The CMOS transistor impedance divides into resistive and capacitive components due to channel resistance and gate ability. In the present work quality factor is being enhanced by reducing the effect of the series resistance (R_s) by pure three-stage common source (CS) circuit.

3 Performance of AI

The conventional AI circuit (Fig.1) is being designed in two different technologies, i.e., 180nm and 90nm CMOS technology. In the proposed circuit two stages are being considered where one stage gives negative transconductance, and another stage provides positive transconductance as shown in Fig.5 for 180nm and 90nm CMOS technology.

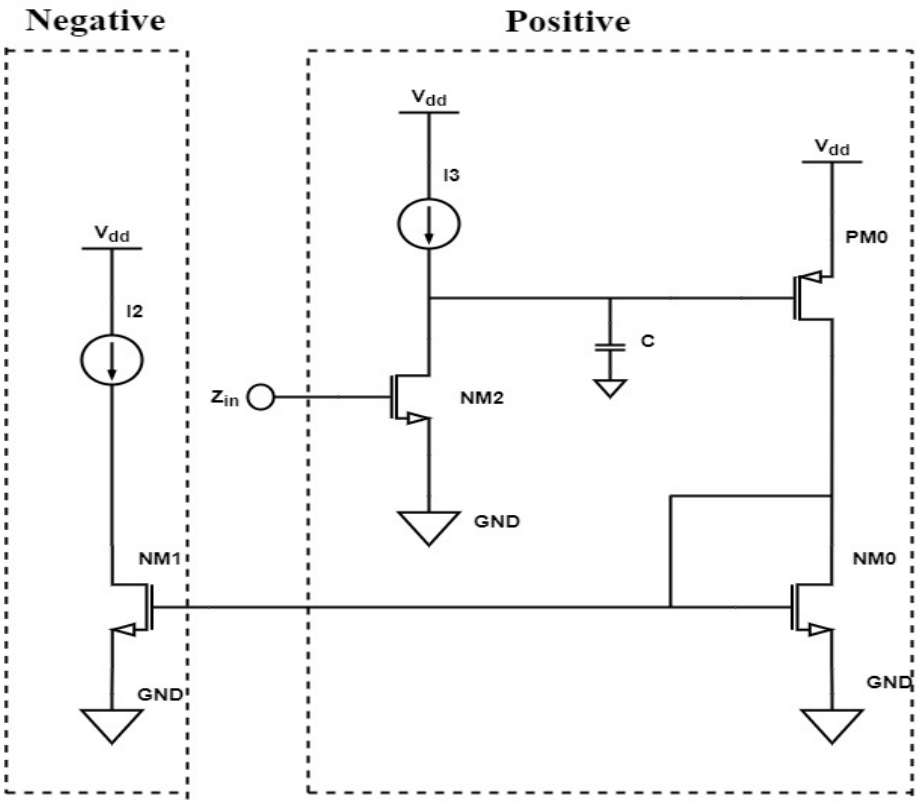

Fig. 5. Gyrator based AI

The data shown in table 1 is chosen in such a manner that all the transistor should be in the saturation region.

Table 1. Proposed circuit transistor data for 180nm and 90nm CMOS technology

Parameters	*180nm*				*90nm*			
V_{dd} *(V)*	1.8				1.1			
Length (L)	180nm				90nm			
Width (w)	nm0	nm1	nm2	pm0	nm0	nm1	nm2	pm0
	2.8u	2.8u	2.8u	5u	4u	4u	4u	4u
Capacitor (c)	100f F				500a F			
I_2	200u A				150u A			
I_3	25u A				100u A			

The Need of migrating from 180nm to 90nm technology is to lessen the feature size of the transistor. The minimal feature size means that during the fabrication process of a transistor, how closely can the transistors be placed on a chip to be used for various purposes. The paltrier the size is, the enormous number of transistors can be assembled on the chip. The number 180nm and 90nm serve the minimum channel length that will be used in fabrication. Also, these numbers are not aimlessly authorized but decided by dividing the previous number by square root of 2 (2 because it is neither too small nor too big). Different technologies are being used today, and the transistor size is shrinking day-by-day to lower the cost of production of a chip as smaller the chip, cheaper is to make it. In the year 2020, the technology has come down to 4nm (approx.). The layout of 180nm technology shown in Fig. 6 and 90nm shown in Fig. 7.

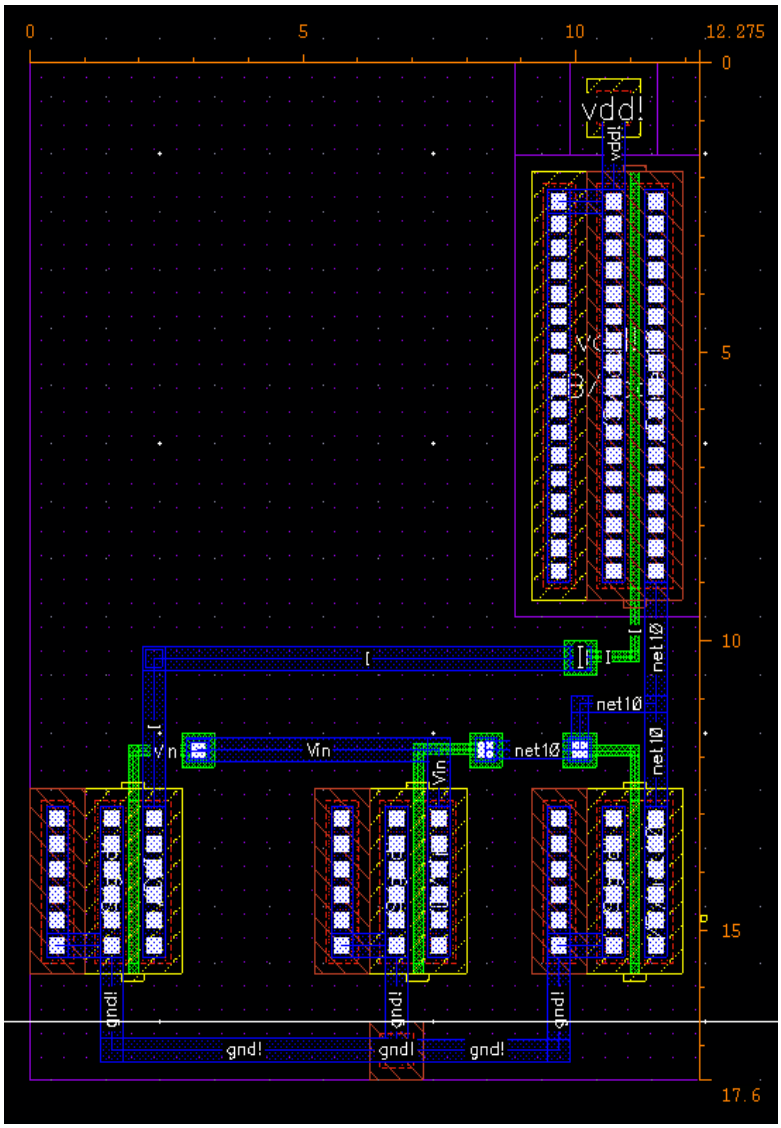

Fig. 6. Layout of AI for 180nm CMOS Technology (216.04μm^2)

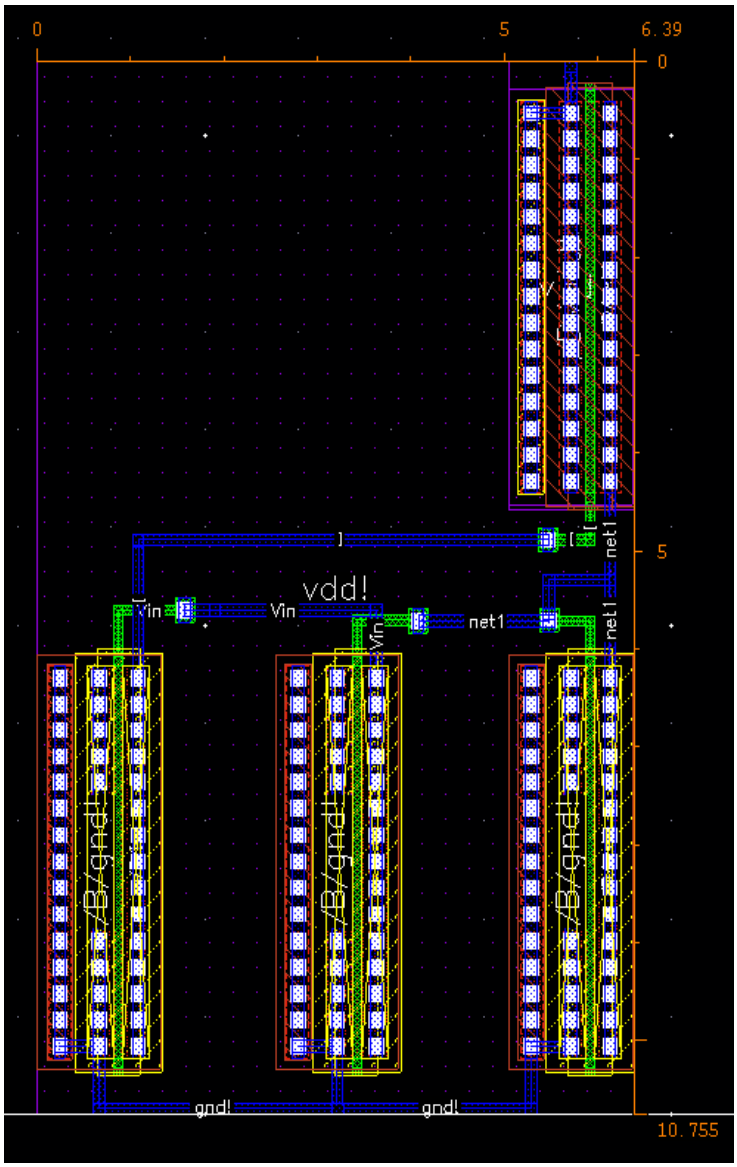

Fig. 7. Layout of AI for 90nm CMOS Technology (68.73 µm^2)

4 Simulation Results

Table 2 shows the comparison of both the 180nm and 90nm AI circuit. When we shrink the technology from 180nm to 90nm performance of the AI enhances the quality factor, power dissipation, area. From the impedance plot (Zin) and phase plot, we can retrieve the quality factor of the AI circuit. A quality factor of AI quantifies the

ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle. Higher the quality factor, lower the resistive term and better-storing capacity. The comparison table of 180nm and 90nm technology are as follows:

Table 2. Comparison of AI circuit for 180nm and 90nm Technology

Parameters	*180nm*		*90nm*	
L (nH)	348 – 3051		40 – 347	
Q_{max}	311 at 478.63MHz		659 at 10.96GHz	
P_{diss} *(mW)*	0.784		0.283	
Area (μm²)	216.04		68.73	
Monte Carlo	50 iterations Min: Z_{in}: 7140Ω Max: Z_{in}: 9450Ω		50 iterations Min: Z_{in}: 7000Ω Max: Z_{in}: 12100Ω	
PVT	Typical Values (P: NN, V: 1.8V, T: 27°C)		Typical Values (P: NN, V: 1.1V, T: 27°C)	
	Process	**Z_{in}(Ω)**	**Process**	**Z_{in}(Ω)**
	FF	51600	FF	4030
	NN	70300	NN	9510
	SS	32500	SS	19400
	Voltage (V)	**Z_{in}(Ω)**	**Voltage (V)**	**Z_{in}(Ω)**
	1.7	59700	1.7	8710
	1.8	70300	1.8	9510
	1.9	81400	1.9	6330
	Temp. (°C)	**Z_{in}(Ω)**	**Temp. (°C)**	**Z_{in}(Ω)**
	-20	34400	-20	5050
	27	70300	27	9510
	74	70300	74	32100

The functional equation for calculation of Quality factor is given by:

$$Q = \frac{Im(Z_{in})}{Re(Z_{in})} \tag{8}$$

From table 2, we can also see that when we shrink the technology, the range of inductance we get also reduced. In contraction to that, we get an enhancement in quality factor, area, power dissipation which can be very useful to use to make more compact applications.

The Z_{in} Plot of 180nm and 90nm technology are shown in Fig. 8 and Fig. 9, respectively.

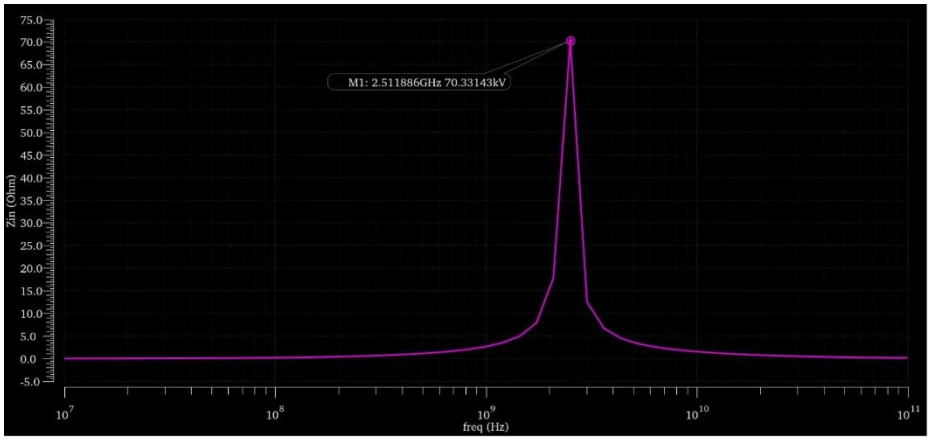

Fig. 8. Amplitude plot of AI circuit for 180nm CMOS Technology

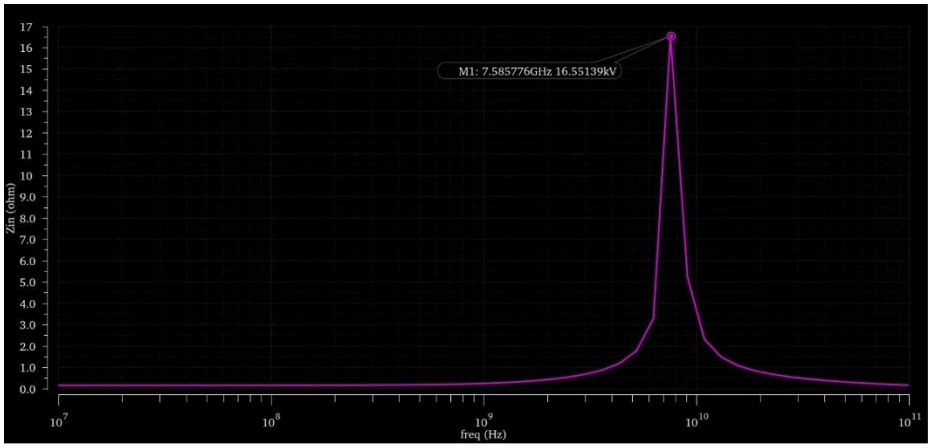

Fig. 9. Amplitude plot of AI circuit for 90nm CMOS Technology

5 Conclusion

The proposed circuit gives us the highest quality factor with lower V_{dd}, high L, low P_{diss}, more excellent inductive frequency range.

The comparison with Ref. [11], [12], [13] is being shown in table 3 for 90nm technology.

Table 3. Comparison of Active Inductor

Parameters	*Ref. [11]*	*Ref. [12]*	*Ref. [13]*	*This work*
$L(nH)$	6.83 – 11.7	1.9	25.7 – 180	40 – 347
V_{dd} (V)	1.2	1.2	1.8	1.1
$P_{diss}(mW)$	22.5	6.4	0.99	0.283
Q_{max}	240	38.8	341	659
Freq. (GHz)	2.4 – 5.35	3.5	0.79 – 2.69	1 – 7.58
Area (μm^2)	-	-	-	68.73

The present work with a better-quality factor is being used in the application like temperature sensor where the sub-threshold proportional-to-absolute-temperature current element strives the Current Control Oscillator (CCO).

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