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FinFET Based Disturbance Free SRAM Cell Design on 45nm Node with the Effect of Line Modulation

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ABSTRACT

In the present scenario, we have great emphasis on high performance and low power in the designing of the memory circuits. The SRAM cell plays an important role in high-performance memory devices. On-chip integration of SRAM, server serious design challenges in terms of cell stability and power dissipation. An 8T SRAM cell at a 45 nm size in Fin-based transistors is proposed to achieve improvement in performance, stability and power dissipation compared with the previous designs for the low-performance circuit. In order to reduce the leakage power, the supply voltage is reduced to the threshold voltage of the cell transistor. This reduction in the threshold voltage of the cell also reduces the Static Noise Margin (SNM) of the SRAM cell. This reduced SNM is responsible for SRAM stability. By employing the proposed 8T circuit, high SNM is achieved in the operation of SRAM memory compared with a CMOS-based 6T SRAM design. In this paper, I propose a methodology and optimize FinFET devices for stable and low-power SRAMs. The 8T SRAM cell provides a much greater enhancement instability by eliminating cell disturbance during read access. The proposed design using FinFET shows less sensitivity to variation and also an improvement of 2.7× in reading static noise margin at V_{DD} = 0.7 V over bulk CMOS based SRAM cell. This paper also shows the effect of line voltage modulation on FinFET based 8T SRAM cells.

KEY WORDS: FinFET, 8T SRAM, stability, cell disturbance, line voltage modulation.

1. INTRODUCTION

To help from speed and area improvements, it is useful to scale the technology of devices [1]. As technology has been scaled down, proportionally leakage current and power in the circuit is increased [2]. The more effective solution to minimize the static power dissipation is to reduce the supply voltage in the subthreshold regions [3]. In this region, MOSFETs suffer from short channel effects. This is due to weak channel control in these transistors, which also leads to increased sensitivity to process variation and voltage modulation [4].

In this paper, the analysis of Static Noise Margin (SNM) has been carried out for the stability of SRAM cells. I propose a simple and the most effective FinFET based 8T SRAM cell and also analyze the effect of line voltage modulation on the stability for this proposed circuit. All the analysis has been carried out on a cadence virtuoso simulation tool at 45nm technology on 27 ^{o}C.

Robust FinFET based SRAM design at 45 nm technology should ensure minimum sensitivity to Scaling of transistors in modern technology.

I. 6T SRAM CELL

Conventional based 6T SRAM cells face many problems while operating at the small supply voltage [5]. In the 6T SRAM cell, variability tolerance is compromised by the contradictory needs of cell read and write ability [6]. Because of the same pass node devices are used to both read and write operation of the SRAM cell. The primary problem in the 6T SRAM cell is that the read and write operations do not perform simultaneously. The SRAM cell having lower read SNM having improved write ability and vice versa. SNM is the capability for the SRAM cell inverters to maintain their state.

2. PROPOSED FinFET BASED 8T SRAM CELL

An accurate and efficient evaluation of FinFET based SRAM cell stability is necessary in the design phase to ensure the correct functioning of the SRAM and to achieve good yield of the cache system.

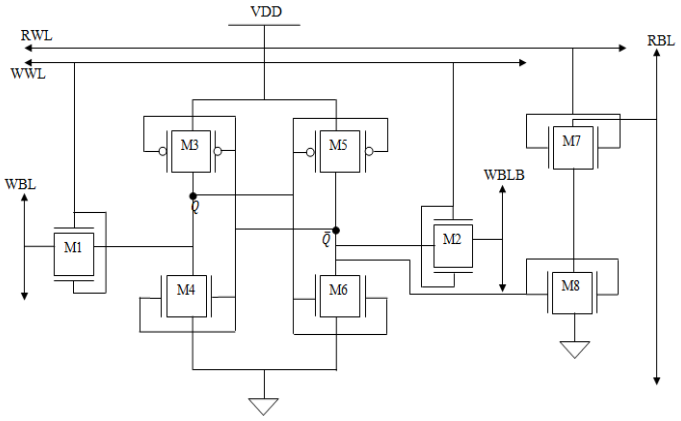

Fig. 1: Proposed FinFET based 8T SRAM Cell.

FinFET devices greatly minimize the device performance variability, due to the fluctuation in the no. of dopant ions, which causes the serious process variability [7]. It is also preferred to extend the 6T SRAM ability together with the novel circuit technique. 8T SRAM cell has been proposed to isolate the read from the write to attain better stability although simultaneously allowing low voltage operation. Fig. 1 shows the FinFET based 8T SRAM cell configuration. Two FinFET transistors (M7 and M8) are added to make disturbance free read operation in the SRAM cell. Since both read and write operations are managed separately.

3. RESULT

Fig. 2 shows the SNM of the conventional based 6T SRAM cell. From this Fig., I calculate the value of SNM which is equal to 287.2mV. Fig. 3 Show that the SNM of the FinFET based 8T

SRAM cell. From this Fig., SNM of the FinFET based 8T SRAM is equal to the 564mV, which is 2.7× of the conventional based 6T SRAM cell. So, a nanometer node FinFET device is suitable for the high-performance circuit.

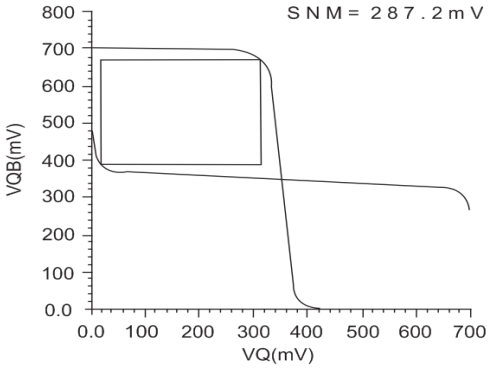

Fig. 2: SNM of Conventional based 6T SRAM Cell.

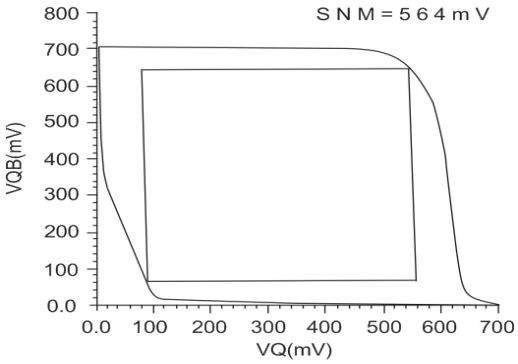

Fig. 3: SNM of FinFET based on the 8T SRAM Cell.

I. Effect of Line Voltage Modulation on FinFET based 8t SRAM Cell

a) Word Line Modulation

The stability of the SRAM cell is also improved by applying the technique using word line modulation at low power supply voltage. This word line modulation method is found in reducing the maximum voltage swing of the word line to preserve the cell access transistor during both read and write operation [8]. Fig. 4 shows the variation between SNM and the word line voltage modulation on a FinFET based 8T SRAM cell. During read operation, SNM of SRAM cells can be improved by reducing the word line voltage.

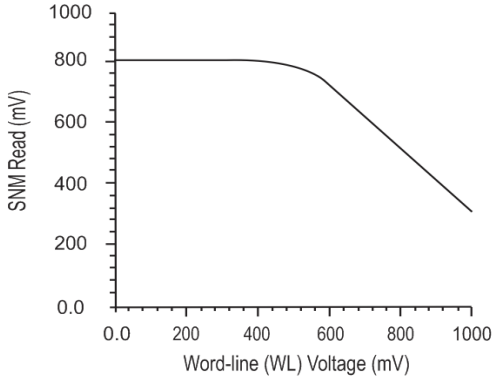

Fig. 4: Word line voltage modulation with read SNM

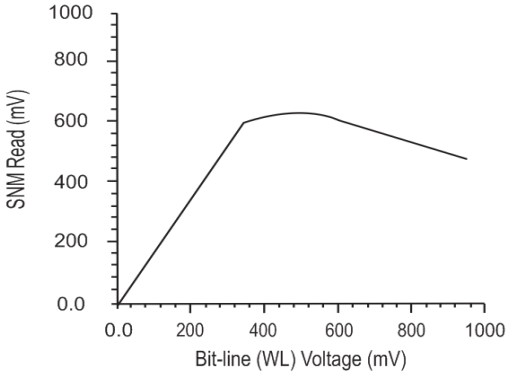

Fig. 5 Bit line voltage modulation with read SNM

b) Bit Line Modulation

Bit line voltage modulation is examined to compute the condition of bit lines at the full power supply voltage. Fig. 5 shows the relation between the SNM of FinFET based 8T SRAM cells and the bit line voltage. From this Fig, it is observed that the Stability is slightly improved by decreasing the bit line voltage compared to the power supply voltage during read operation. This reduction in bit line voltage also allows for read mode SNM improvement without any modification of the SRAM cell array design [8]. So, from this analysis we can show that at 45 nm technology, stability can be improved by reducing the word-line voltage and bit line voltage during read operations with respect to supply voltage.

4. CONCLUSION

In this paper, the 8T SRAM cell as proposed in this work is particularly attractive for high performance array design and provides the write ability compared to the conventional based 6T SRAM cell. To verify the proposed SRAM cell, a 32kb SRAM block using the proposed FinFET based 8T and conventional 6T SRAM cells were designed. The simulation results discussed above, Improve the Read SNM of FinFET based 8T SRAM cells. SNM can be improved by adjusting the device parameter of the FinFET based 8T SRAM cell without requiring any modification of the SRAM cell.

ACKNOWLEDGEMENT

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