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FPGA Based Voting Machine

Mritunjay Kumar, Gurpreet Singh Dhami and Ravi Shankar

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Mritunjay Kumar
School of Electronics and Electrical Engineering
Lovely Professional University
Phagwara, India
mkbgs0123@gmail.com

Gurpreet Singh Dhami
School of Electronics and Electrical Engineering
Lovely Professional University
Phagwara, India
dhamicherry123@gmail.com

Ravi Shankar
School of Electronics and Electrical Engineering
Lovely Professional University
Phagwara, India
ravi.14909@lpu.co.in

***Abstract*— Electronic Voting Machine (EVM) is used in our country for Elections. It consists of two units (1) a control unit (2) the balloting unit. Balloting unit has the names ofcandidates via labeled buttons and the control unit is used for counting the votes. This method is very complex in its own and it is being used in the country from thelast 8-9 years. In this research paper, we have implemented the Electronic Voting Machine by using FPGA. This is a new method that can be used in Elections that happen in the country. ThisVoting Machine is designed as a application of VLSI and understanding the futurescope of VLSI in real-time applications. It is designed to overcome the disadvantages of Electronic Voting Machine. These types of Voting Machines are more safer and easy to use , this will overcome the booth capturing process in rural areas.**

***Keywords*— FPGA, Xilinx tool, Verilog, Electronic Voting Machines, Vivado tool**

I. INTRODUCTION

Electronic Voting Machine (EVM) is being used in the Indian elections for the very long time. This method of Electronic Voting Machine is still used in the country for the elections. This method is efficient and good to go but it doesn't provides the safety because in many of the cases booth-capturing is there and it leads to unfair results [13]. To defeat the opposition party the ruling party take wrong planning and this may cause a bad election and bad impression of the country. To overcome this problem, we have come up with a different idea which leads to fair voting system in the country [5]. If We see take the India as a refrence then we see there are total 900 million people are eligible to vote [6], and for fair election we need safe and portable voting machine which is more compact and safe. This paper dispenses the design of the Electronic Voting Machine EVM by using a digital technique which is secure, safe and error-free. This paper mainly aims at the designing of a Voting Machine by using FPGA which is basically known as Field Programmable Gate Array. This design is totally based on the concepts of VLSI and the paper shows that how the concepts of VERILOG can be used to implement a real-time application [8]. This paper proposes an Electronic Voting Machine in Verilog by using Vivado 2019.1. Since we proposed to understand that it is hard to manage the whole voting process with ballet paper and so on.

Hence we have designed the ballet machine using VERILOG HDL with Vivado tool which can done on FPGA (Field Programmable Gate Array).

II. Literature Survey

In [1] paper, we can see that Soomro, Z. A mentioned that the ElectroMechanical Devices are better as compared to paper ballet boxes for recording votes .In Manual voting the chances of corruption is high like booth capturing ,fake casting of votes and so on .The Electronic Voting system has high accuracy , safe and reliable .

Ziad, M. T. I., Al-Anwar [4] intimated in their review papers that previous years the voting is done on ballet paper and this is not safe but after some years when EVM's came into the market with the fact that it is safe and reliable and after some time it also got hacked, so the fact is that we need change in Electronic Voting Machines also.As we see the for any country the voting is important part of any country overall development so in large democratic country a fair election should be introduced . So, there are lot of voting machines and voting techniques available in the market and we have reviewed so many research papers and then we came up with this FPGA voting system solution. In fact this system is very much safe and easy to use and we can make a election more fair and free from all disruptions.

In research paper [8], we can see that the voting machine can be authorized by the fingerprint also, as we all are aware of the aadhar authentification , in voting process aadhar i.e the identity of a person is definitely checked by the booth member, and once they get verified then are allow to vote.But in FPGA based voting machine we can authorize once identity with the voting machine itself so when they automatically get verified and eligible to vote . There is no need of third member between the voter and voting machine.This may definitely leads a fair election and a fair environment.

In every election one major problem with the election is cyber attack which includes the online fraud of electronic voting machine. In the [8], research paper we can read that Reddy G.S has raised the security concern of voting machine

In the [8], research paper we can read that Reddy G.S has raised the security concern of voting machine . He and his team also includes that the as the machine is electronic and we are authorizing with online verification so it's very risky to save someone's data. In this proposed system i.e FPGA Based voting machine we can fetch someone's data very easily.

Hossain, T [10], initiated in their paper that to overcome of these difficulties and build the electric model method a good one, creation of electronic mechanical device in digital field is provided on that paper , it's difficult to interfere votes in online field and provides a relaible, safe and secure technique for conducting elections described in their paper that the old and previously choice of voting was terribly long and difficult method and extremely inaccurate and unsafe. Polling by Electronic Voting Machine (EVM) may be a good, safe and absolute nice technique that takes less your time. Currently this electromechanical device (EVMs) used in lok sabha , vidhan sabha and an assembly election accepts one vote from the citizen of their respective country. However in elections like gram panchayat wherever every citizen casts their votes to one candidate, their choice machines didn't work easily. So, as we see that the major elections that are happening in any country and the solution we are providing is totally safe more reliable than any other voting machine available in market . We are creating a FPGA voting machine which will solve the most problem related to the voting machine in the market.

Oksuzoglu, E., & Wallach, D. S[16], illustrates that a voting machine can be portable also like nano votebox which is portable and useful to carry everywhere safely , this machine will create a huge impact on the society for smaller SOCIETIES elections. Basically we can create and use the voting machine as per our need , there are lot of FPGA available in the market which are nano, medium and large . We can create the voting machines with the help of these technologies.

As long as world is growing , population increases rapidly throughout the world especially India which includes the population approx. 140 million. By the increasing population there voters will also increase . And for fair and secure election we need some fair electronic voting machines which leads secure and good election environment and this Xilinx FPGA based voting machine definitely solve these problems for sure . In [11] research paper it is mentioned about the elections and voting machines and everything.

III. Proposed System

This Voting Machine is implemented on the FPGA NEXYS-4 board .The overall design looks like votes given to 4 different candidates. The first 4 switches in FPGA board represents the votes given to each of the 4 individual's. Then there is a reset button which will reset the whole system. Then there is a mode button which will ensure the safety of the Voting Machine. People can cast votes to the specific candidates only if the mode button is set to **0**. If the mode button is changed from 0 to 1, then the votes cannot be casted, only the counting of the voteswill be done. Here, we have introduced a new concept which is known as Valid Vote. Valid Vote is the vote received by the candidate when the switch is pressed for a time duration of 1 second. When the valid vote is casted then the LED's of FPGA will glow which ensures that a fair vote has been casted. If the switch is pressed for less than 1 second, then it will not be counted as a vote.

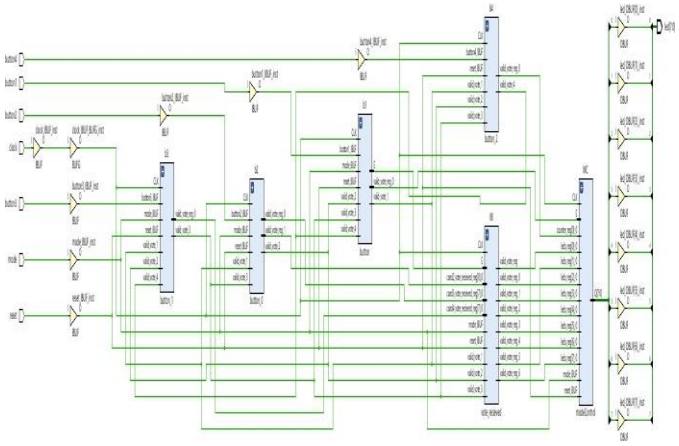
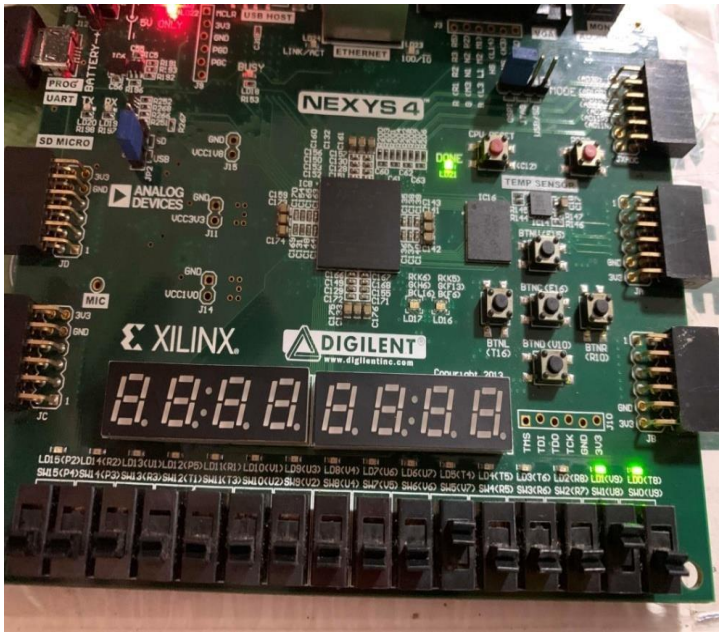


Figure 1. *Schematic Diagram of FPGA EVM*

The Voting machine is implemented on NEXYS-4 FPGA board. The FPGA hasfollowing properties : It has 16 user switches and 16 user LED's where we can give our own set off inputs. Nexys-4 has two 4-digit 7-segment displays and two tri-color LEDs.12-bit VGA output and PWM audio output .Micro SD card connector, PDM microphone, 3-axis accelerometer ,Temperature sensor, 10/100 Ethernet PHY,128MiB DDR2, Serial Flash, Four Pmod ports. Digilent USB-JTAG port for FPGA programming and communication. On-chip analog-to-digital converter (XADC).



The below figure 2 depicts the schematic of the proposed electronic voting machine with input and output signals. Elements that are used to connect input and output ports of a module instantiation together with some other element are called wires.
The default values of wire is ‘Z’.

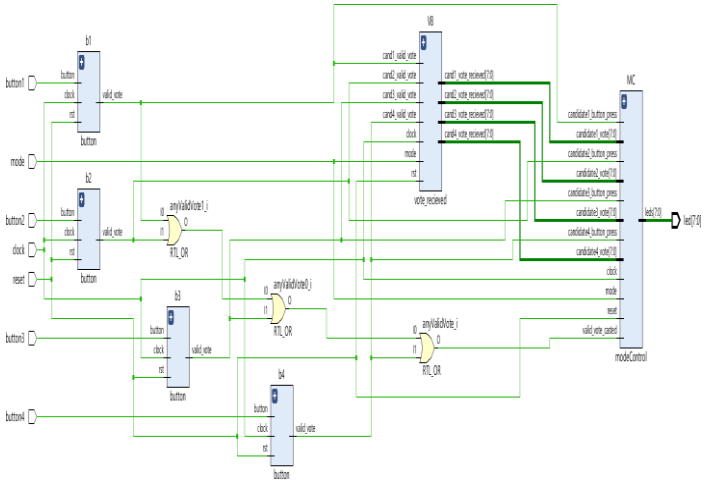


Figure 2 .Schematic view

Here the input pins are button1, mode, button2, clock, reset, button3, button4 respectively. The output pin is declared as led which is of 8 bits . Here the wires are declared as (valid_vote_1, valid_vote_2, valid_vote_3, valid_vote_4),and,(cand1_vote_recieved,cand2_vote_recieved, cand3_vote_recieved, cand4_vote_recieved).The votes to each candidate is given through the switches that are there in the FPGA Board.

Concept of Clock Divider

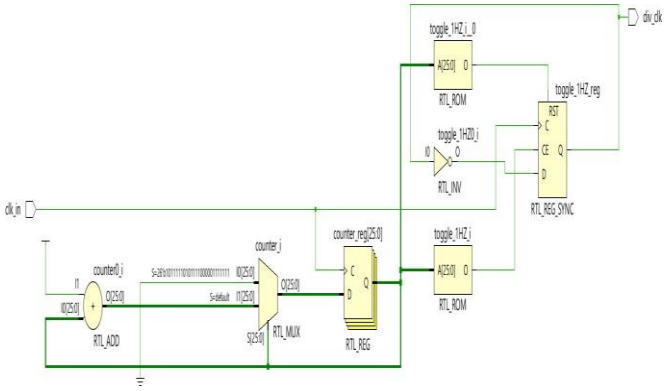


Figure 3. clock divider

A clock divider is a circuit which is used to divide the frequency of the input clock. A clock divider circuit creates lower frequency clock signals from an input clock signal. The divider circuit counts input clock cycles, and drives the output clock low and then high for some number of input clock cycles. Clock divider is very much essential while working on FPGA because we need to see the small changes and if the clock will be kept high, then the small changes will not be seen. So in our Electronic Voting Machine, we have used Clock divider by 2 as shown in figure 3.

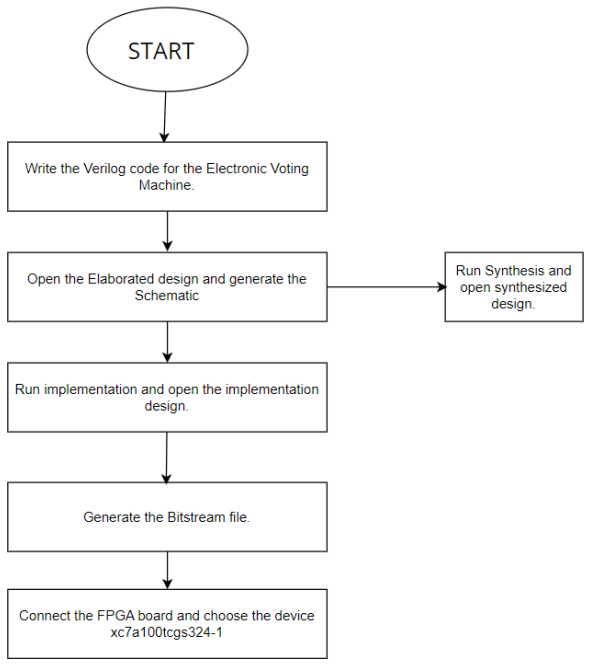
In this case, we have divided the incoming clock frequency by 2 as shown in figure 4.

```
module clk_div(clk_in , div_clk );
input clk_in ;
output div_clk ;
parameter  count_clk = 50_000_000 ;  ///100MHz/2 = 50MHz
reg [25:0] counter ;
```

Figure 4.clock frequency

Procedure to use the Electronic Voting Machine:

Set the reset switch to high so that all the information that is stored by default is erased. Now for casting the votes, the mode button should be kept low i.e. logic 0 . While casting the votes to each individual the reset button should be kept low i.e. logic 0. When a valid vote is given to the candidate, then LED's will be on for 1**s**econd which shows that the vote has been given. Once the voting is done, then we have to count the number of votes received by a particular candidate. So we have to change the mode from 0 to 1. If we want to see the number of votes received by a particular candidate, then we have to make the respective button on.



Simulation Results and Discussion:

- Whenever a valid vote is casted , the LED is on for a duration of 1sec .
- The counting of total votes can only be done when the mode button is kept to 1.
- The concept of valid vote restrict people to cast multiple votes.
- To reset the system, after the counting of the votes is done the reset button is set to 1
- The counting of the votes can be done through the FPGA board.

IV. Conclusions

The Electronic Voting Machine is successfully implemented on FPGA. Whileimplementing, all the concepts of VLSI has been used. Now this prototype is thoroughly tested and it is working as per the specifications. NEXYS-4 FPGAboard and Vivado 2019.1 is used in the implementation. This Voting Machine is now ready to be used in real Indian Elections.The advantages of FPGA based Voting Machine includes: It is a very compact design and easy to transport from one election center to the other. It works very efficiently and is error- free. It is very much safe and secure and it is not time- consuming method. A new concept of Valid Vote is introduced in this Electronic Voting Machine.

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