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# Performance Analysis of CMOS Inverter Using Sleepy Stack Power Dissipation

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# PERFORMANCE ANALYSIS OF CMOS INVERTER USING SLEEPY STACK POWER DISSIPATION

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***Abstract* - Scaling using the CMOS inverter techniques has improve performance and reduce power dissipation Two important characteristics of CMOS devices are high noise immunity and low static power consumption. In nanotechnology the power dissipation and various performance analysis have emerged as major design considerable. These may grow the problem continue with leakage power and become a fundamental problem of power consumption. To overcome the issue of deep submicron technology by seeing the report of to International Technology Roadmap for Semiconductors (ITRS), the total power dissipation may be significantly contributed by leakage power dissipation projected to go exponentially in next decades.to survey that support good performance, low dissipation in era of low consumption. Sleepy stack approach is a combination of two well-known low-leakage techniques: the forced stack and sleep transistor approach is very less as compared to other techniques. This paper represents performance analysis of CMOS inverter using sleepy stack power dissipation consume 50% less power as comparison to standard CMOS technique in 60nm technology**

***Keywords* — CMOS Inverter, Power dissipation, Leakage power , forced stack, sleepy stack ,low-power pipelined cache.**

## I. INTRODUCTION

As we know the high-performance circuit needs the large number of transistors with high speed. But this improvement in the performance comes with power dissipation. And the major demand in VLSI technology, small power consumption as compared to discrete components circuit. As the technology is getting finer, the percentage of leakage power dissipation in total power dissipation is increases significantly. There are two main sources of power dissipation in any processors are static power and dynamic power. This static power dissipation causes due to flow of leakage current. The leakage current is defined as the current standby or sleep mode. And other power dissipation is dynamic power dissipation which is the power dissipation in CMOS circuit in active mode. Leakage power dissipation depends on the gate oxide thickness, gate size and threshold oxide thicknesses are the very important parameter for leakage power dissipation.[1]. For the high performance and low power consumption results the transistor size and the scaling is required [2] Using such sleepy stack technology, the leakage power require ultra-low leakage power consumption and are willing to pay some area and delay cost and retains the original state high-Vth. One of the most effective dynamic power reduction techniques is lowering the supply voltage of CMOS transistors because the power consumption of CMOS transistors increases quadratically proportional to the supply voltage. However, lowering the supply voltage incurs an increase in transistor switching delays. Therefore,2 designing CMOS circuits typically necessitates trade-offs between performance (in terms of delay) and power consumption. Although CMOS circuits are governed by such trade-offs, it is possible for a system to selectively lower supply voltage without compromising performance at the architectural level. The strategy is to lower supply voltage for circuits in non-critical paths while maintaining supply voltage for circuits in critical path(s); thus, available surplus slack in non-critical paths is removed. In our particular case, we observe that by pipelining the caches, we can obtain large surplus slack, which allows for large dynamic power savings. This new low-power cache technique is named Low-Power Pipelined Cache (LPPC). By apply sleepy stack instead of lowering supply voltage, LPPC can be used to save leakage power consumption.

## II. SLEEPY STACK APPROACH

Gate terminals of both NMOS as well as PMOS transistors are tied together and connected to a single source which serves as input for the inverter. SLEEPY STACK APPROACH the sleep and stack approaches. The sleepy stack technique divides

existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. It having the benefits of both stack and sleep techniques are used simultaneously in the sleepy stack approach. (1) During the sleep mode, sleep transistor is turned ON and stacked transistor suppress the leakage current while saving the state. Each sleep transistors are placed parallel to one stack transistor which reduces the resistance of both transistor and thus delay is decreased during active mode. (2)When sleep transistors are turned OFF, the existence path from $V_{dd}$ or ground prevent the float in output and also in this case, leakage current further can be reduced by applying high threshold voltage on the sleep transistor and the transistor in the parallel to the sleep transistor.(3)In this approach, pull-up network is replaced by three transistor and similarly pull-down network is also replaced by three transistors and also additional wire is connected for S and S' which are sleep signal. (4) During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. This approach since every transistor is replaced by three transistors and since additional wires are added for S and S', which are sleep signal

## II. DIFFERENT TYPES OF POWER DISSIPATION

- The total power dissipation in a CMOS circuit can be expressed as the sum of three main components:
- Static power dissipation (due to leakage current when the circuit is idle)
- Dynamic power dissipation (when the circuit is switching)

### *2.1 REDUCE POWER DISSIPATION*

- Short circuit power dissipation
- Sleepy stack approach

## IV. DIFFERENT PERFORMANCE ANALYSIS

### *4.1 CONVENTIONAL CMOS INVERTER APPROACH*

Conventional CMOS inverter approach. In the conventional CMOS inverter approach, pull-up network and pull-down network are used with two transistors. The pullup network is called a PMOS transistor and pull-down network is called a NMOS transistor. Its operation can be understood with a simple switch model. The CMOS inverter transistor is nothing more than a switch with an infinite off resistance and a finite on-resistance. When input is logic 0, logic 1 is obtained at the output and when input is logic 1, logic 0 is observed at the output. CMOS inverter has three components of power – static power, dynamic capacitive power and dynamic short circuit power Conventional CMOS inverter approach. In the conventional CMOS inverter approach, pull-up network and pull-down network are used with two transistors. The pullup network is called a PMOS transistor and pull-down network is called a NMOS transistor. Its operation can be understood with a simple switch model. The CMOS inverter transistor is nothing more than a switch with an infinite off resistance and a finite on-resistance. When input is logic 0, logic 1 is obtained at the output and when input is logic 1, logic 0 is observed at the output. CMOS inverter has three components of power – static power, dynamic capacitive power and dynamic short circuit power. Power dissipation in the circuit is defined as the rate at which the energy is taken from the source and is converted to heat. There are three main types of power consumption in CMOS circuits: leakage power, short circuit power, and dynamic power. 1) Leakage Power: The leakage power is static, and it is mainly determined by the current flowing through the channel when the transistor is off, which is generally very small. The technique leakage power is given as:

$$P_{LEAKAGE} = VDD \sum^{N}_{I=} I_{DSi}$$

Where is the current flowing through the channel in the $I_{th}$ transistor.

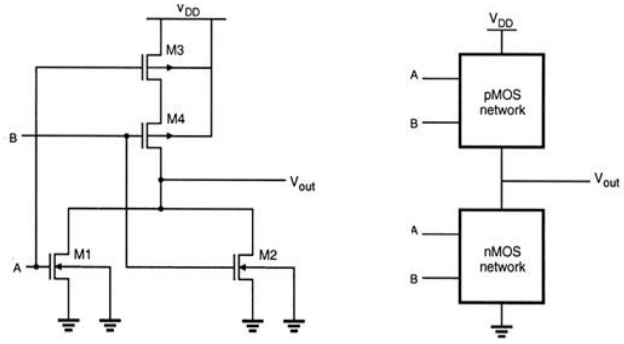



Fig:1 conventional CMOS inverter

### *4.2 FORCED NMOS APPROACH*

This approach is same as conventional CMOS but with an added NMOS at the bottom. The two NMOS devices increase the delay which results in reduction in leakage power in the circuit. An extra NMOS decreases. The$I_{dd}$ through mos device.hence decreasing power consumption as compared to the conventional CMOS

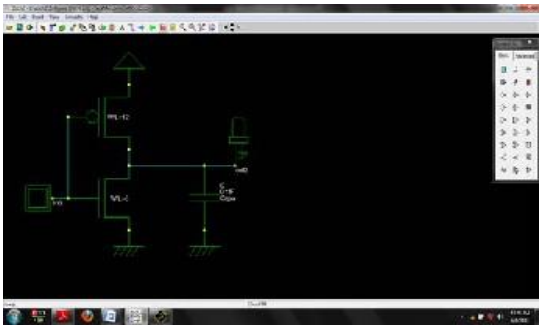
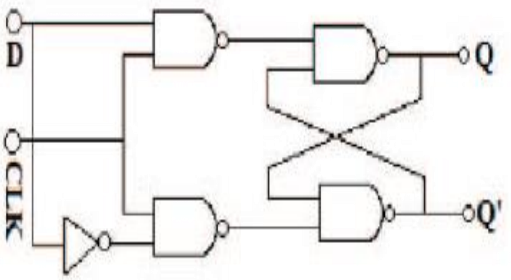


Fig.2 shows NMOS Technique .IJSER © 2013 http://www.ijser.org

### *4.3 FORCED 2 NMOS*

This approach combines property of both reduce swing as well forced NMOS inverters. The load PMOS transistor in the reduced swing inverter is always in saturation since Vgs =Vds . It reduces the voltage at the source of the second pMOS in each inverter to approximately Vdd -Vtp thus switching it off when the low-swing clock signal reaches its peak voltage. This approach has low power consumption but with increased de- lay and layout area.The output voltage swings from 0 to V dd - Vtp . PMOS acts as a load hence reduces voltage swing to Vdd - Vtp- This reduction in swing results in a reduced in power consumption.



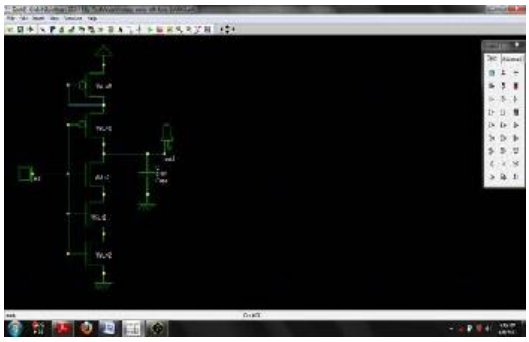



Fig:3 Forced 2NMOS layout

### *4.4 Stack Approach*

Another scheme for reducing leakage power is the stack approach, which uses a stack effect by breaking an existing transistor into two half size transistors to take advantage of the stack effect [4]. It is based on the principle that a PMOS and NMOS device can be replaced by two equal NMOS and PMOS devices of half W/L .Gate terminals of both NMOS as well as PMOS transistors are tied together and connected to a single source which serves as input for the inverter. Output is taken across a capacitor which serves as a load for the inverter circuit. However, divided transistors increase delay and could limit the usefulness of this approach.Fig.2 shows the stack technique.

### *4.5 D FLIP FLOP CIRCUIT*

Leakage Power Analysis When we reduce the channel length or provide scaling so the leakage power is increase, Leakage power provides standby power of any device. Leakage power association to CMOS D-Flip Flop among SVL and customized SVL is given in beneath

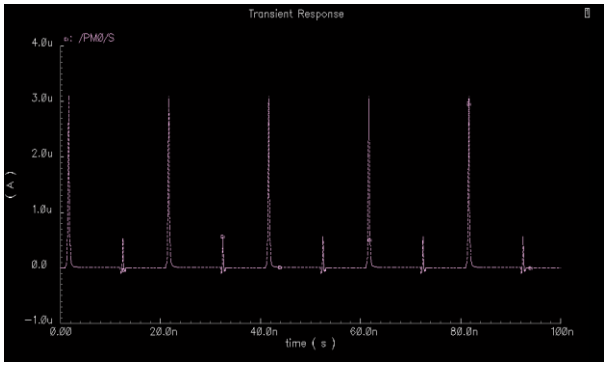
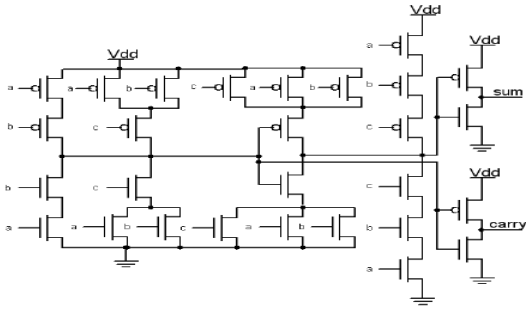



Fig.4 Leakage current may be occurs from substrate injection belongings and sub-threshold voltage in D flip flop.

Leakage power is wastage of power supply and leakage power of Schmitt trigger is $P_{LEAK} = I_{LEAK}V_{dd}$ Where $P_{LEAK}$ is leakage power of CMOS D-Flip Flop, $I_{LEAK}$abbreviated for leakage current, $V_{dd}$ is power supply.

### *4.6 Full adder circuit*

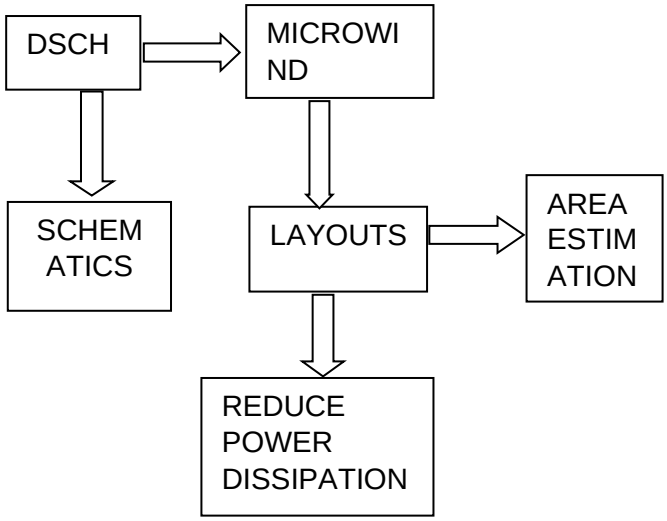
Sum and Carry out are outputs and A, B and $C_{in}$ are inputs. It has 28 transistor full-adder also known as Mirror full-adder. This is an efferent way implement of generate/propagate/delete function of full adder. As depicted in fig 1. $C_{out}$ is set and $V_{dd}$ is GND Either delete or generate is high respectively.




$C_{out}t = AB + BC_{in} + AC_{in}$ (1) Sum = $C_{out}(A + B + C_{in}) + ABC_{in}$

## *V. EXPERIMENTAL DESIGN*

For experimental investigation of all CMOS inverter techniques, two types of software tools are used. Figure 7 shows experimental methodology. For schematic purpose DSCH has been used and for layout designs MICROWIND has been used. Schematic circuit and layouts are design for all type of CMOS inverter approaches. Schematic are used for to make a different type of digital and analogue circuit and all the parameter are estimated with the help of MICROWIND window where the layout is design. These parameters are power dissipation and layout area at different technology of all considering approach. Schematics are designed for all considered techniques using schematics editor i.e., DSCH Window in MICOWIND software tool targeting TSMC are used to obtain net lists of the circuits and the net lists are used to simulating purpose. Inverter based on conventional CMOS, forced NMOS, forced PMOS, forced 2NMOS, stack approach and sleepy stack approach are designed and simulation results have been taken in terms of power dissipation and layout area.




*Block diagram of sleepy stack CMOS analysis*

## *VI. SUMMARY RESULT*

As the circuit shows analysis of CMOS inverter using sleepy stack approach by apply different supply voltages have been considered at different technologies.

Table 1 SHOWS THE VALUE OF SUPPLY VOLTAGES AT DIFFERENT TECHNOLOGIES.

| **Technology** | **45 nm** | **65 nm** | **90nm** | **120nm** |
|---|---|---|---|---|
| Vdd | 0.4 v | 0.7v | 1.2v | 1.2v |

Simulation results have been carried out for all techniques at different technologies from 45 nm to 120 nm. Table 2 shows power dissipation in all techniques at different technologies. As the technology scales down, power dissipation in all techniques reduces because of applied supply voltage. From the table 2, it is observed that power dissipation in sleepy stack technique is minimum as compared to all techniques. In 65 nm technology, power dissipation in sleepy stack technique is μw, which is 47.6% less as compared to conventional CMOS technique.

Table 2 POWER DISSIPATION USING DIFFERENT TECHNIQUES

| **Techniques** | **45 nm (µw)** | **65 nm (µw)** | **90 nm (µw)** | **120 nm (µw)** |
|---|---|---|---|---|
| Conventional CMOS | 0.08 | 0.373 | 1.546 | 2.859 |
| Forced NMOS transistor | 0.075 | 0.333 | 1.251 | 2.451 |
| Forced 2 NMOS transistor | 0.070 | 0.300 | 1.00 | 2.001 |
| Full adder | 0.65 | 0.275 | 0.75 | 1.75 |
| D flip flop | 0.58 | 0.255 | 0.72 | 1.68 |
| stack | 0.51 | 0.199 | 0.68 | 1.58 |
| Sleepy stack | 0.045 | 0.189 | 0.664 | 1.0 |

## *VII. CONCLUSION*

As the sleepy stack is best power analysis source technique in the static mode. So, the proposed circuit has designed to reduce the power dissipation in this paper, performance analysis of CMOS inverter circuit has been done using standard CMOS technique to sleepy stack technique. Other inverter techniques are forced NMOS, forced 2 NMOS, Full adder, D flip flop and stack approach are also analyzed. Schematic circuit design and Layout design of inverter using all techniques have been done in DSCH and MICROWIND tool. Power dissipation have been calculated for all techniques. It is concluded that power dissipation in sleepy stack approach is very less as compared to other techniques but the area increases due to a greater number of transistor count. Power dissipation in sleepy stack approach is 50% less as compared to conventional CMOS technique in 60 nm technology

## *VII. ACKNOWLEDGMENT*

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