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№ 8859

Current Sharing Control Method for Parallel Three-Level Inverters Based on PSST Strategy

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September 22, 2022

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***Abstract*—Communication equipment is often utilized in conventional parallel inverters current sharing, which will result in limited equipment arrangement and communication line freedom. In this paper, current sharing control method for parallel three-level inverters based on power/signal synchronous transfer (PSST) strategy is proposed. A mathematical model based on SVPWM control method is established for NPC type parallel three-level inverters, and the stability of the system is analyzed. On this basis, the PSST technique is introduced to convert the output current of the master inverter into a rectangular carrier signal carrying information, which is then transmitted to the slave inverter as its output current reference, realizing the parallel inverter current sharing. Finally, simulation results verify the feasibility and effectiveness of the control method.**

Keywords—Master-slave control, Parallel inverter current sharing, PSST

I. INTRODUCTION

With the increase of various power-using devices, the single inverter power supply systems are difficult to meet the requirements, so it is necessary to use inverters in parallel to solve the problem of insufficient output power of individual inverters [1]. However, the consistency of output voltage amplitude, phase and other indicators of each subsystem need to be considered in the parallel inverters power supply design. Large loop current will be generated if the output voltage is not synchronized, leading to the current imbalance between the inverter bridges, low total output current and high additional power loss [2].

Power sag control method [3,4,5], distributed control [6,7], and master-slave control [8,9] are the main current sharing methods for parallel inverters operating. The power sag control method has the advantages of simple system structure and no communication lines, but sag characteristics introduced artificially will lead to poor output external characteristics of the system, and the amplitude and frequency of the output voltage deviate from the rated value at steady state. Interconnect lines were used for distributed control, which allows information interaction between subsystems to achieve a redundant inverter system, but the use of interconnect lines increases the complexity of the hardware and reduces the reliability of the system. Master-slave control features simple equalization control circuit, high accuracy of equalization and excellent dynamic performance, but its reliability and freedom of equipment arrangement are limited by communication lines. In [10], a new master-slave control strategy was proposed, by adopting the sag-controlled inverters as master units and the remaining inverters as slave units using PQ control, which realizes automatic power regulation and system frequency-voltage recovery, however, the sag control and master-slave control are both introduced in the control strategy, resulting in a complex control method and still requiring communication lines for information interaction; A new strategy is proposed in [11], by designing current reference low-pass filter and adding voltage feedforward link in the slave module, which maintains good transient performance, compensates the effect of low bandwidth communication, and achieves stable and robust operation. However, bluetooth and other wireless communication devices have low bandwidth and low rate, which can lead to large communication delays and poor system transient performance; For sudden load changes and module failure operation in parallel inverters, a democratic master-slave control method based on CAN bus strategy is proposed in [12], by reducing the use of interconnecting lines, the output voltage quality is improved and the high reliability operation of the system is ensured. The master-slave based control current sharing controls for parallel inverters focus on multiple control synergies, design control parameters analysis, and etc., but lack the solution to the problem of interconnection line dependence in information inter-action.

In [13,14], the power/signal synchronous transfer (PSST) theory is applied to DC/AC converters. Therefore, a new current sharing control method for parallel three-level inverters based on PSST strategy is proposed in this paper. In section II, the mathematical model of NPC-type shunt inverter and the system stability are analyzed. On this basis, the power signal synchronization transmission strategy is introduced, in which the output current of the master inverter is converted into a binary baseband signal for transmission in the power circuit, and the signal carried by the demodulated load voltage from the inverter is taken as its output current reference, thus realizing the master-slave control strategy of the parallel inverter without interconnection lines. Finally, simulation results are presented in Section III.

II. PARALLEL THREE-LEVEL INVERTERS CURRENT SHARING BASED ON PSST STRATEGY

A. System modeling and stability analysis

In this paper, the NPC-type three-level parallel inverter is studied, whose controller can be seen as a rectangular carrier signal carrying information, while the power circuit becomes a communication channel with low-pass characteristics, transmitting the carrier signal generated by the source. As the master and slave inverters are structurally identical, for the purpose of subsequent controller design, the mathematical model is constructed for the master inverter only. A typical three-level voltage-source inverter is shown in Fig. 1.

In Fig. 1, V_{dc} is the dc bus voltage; u_{aN}, u_{bN}, u_{cN} are the phase voltages of the inverter bridge output with respect to the

This work was supported by the National Natural Science Foundation of China under Grant 51977208.

load neutral; i_a is the filter inductor current; i_C is the filter capacitor current; R is the inverter load.

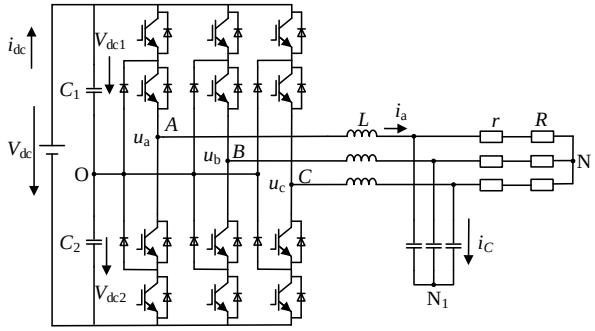

Fig. 1. Three-level three-phase bridge inverter main circuit topology

By defining the switching function, each switching tube in the circuit can be replaced by a single three-throw switch. The switch is on when the switching function $S(t)=1$, and off when the switching function $S(t)=0$. Then the KVL and KCL equations can be listed according to the topology of the main inverter in Fig. 1.

$$\begin{cases} L\dfrac{\mathrm{d}i_a}{\mathrm{d}t} = v_{AO} + v_{ON} - e_a \\ L\dfrac{\mathrm{d}i_b}{\mathrm{d}t} = v_{BO} + v_{ON} - e_b \\ L\dfrac{\mathrm{d}i_c}{\mathrm{d}t} = v_{CO} + v_{ON} - e_c \end{cases} \tag{1}$$

In (1), v_{ON} is the voltage value between the midpoint of the dc-side voltage and the midpoint of the three-phase grid. Since switching functions are featured by discontinuities, the mean state space method is adopted to eliminate the discontinuities, and then coordinate transformation is carried out, and finally a mathematical model of the three-level NPC inverter with two identical step rotating dq coordinate systems is obtained as shown in (2). In this case, the system becomes a two-phase linear system, which facilitates the design and study of the control system.

$$\dot{X} = BX + DE \tag{2}$$

In (1), matrix B represents

$$B = \begin{bmatrix} 0 & \omega & \dfrac{S_{dp}}{L} & -\dfrac{S_{dn}}{L} \\ -\omega & 0 & \dfrac{S_{qp}}{L} & -\dfrac{S_{qn}}{L} \\ -\dfrac{S_{dp}}{C_1} & -\dfrac{S_{qp}}{C_1} & 0 & 0 \\ -\dfrac{S_{dn}}{C_2} & -\dfrac{S_{qp}}{C_2} & 0 & 0 \end{bmatrix}$$

matrix X represents

$$X = [i_d \quad i_q \quad V_{dc1} \quad V_{dc2}]^T$$

matrix D represents

$$D = diag\left[-\frac{1}{L} \quad -\frac{1}{L} \quad \frac{1}{C_1} \quad -\frac{1}{C_2}\right]$$

matrix E represents

$$E = \begin{bmatrix} e_d & e_q & i_{dc} & i_{dc} \end{bmatrix}^T$$

In this paper, a modified master-slave control method is adopted to control the parallel inverters, giving full play to the advantages of good power quality and high stability in microgrid applications. The master inverter is used to stabilise the bus voltage of the system, and the output current of the master inverter is sent to the slave inverters through the PSST strategy, which is used as a reference for the output current of the slave inverters, so that the output power of each inverter is proportionally distributed, thus the loop current in the microgrid is suppressed. The system structure is shown in Fig. 2.

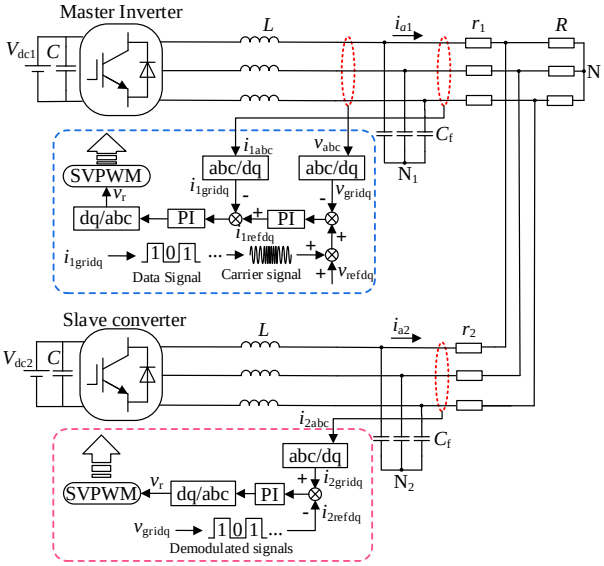

Fig. 2. Parallel inverter system structure

Voltage and current double closed-loop control is used for the control loop of the main inverter, and the voltage model in the dq coordinate system in (2) is simplified. Let

$$\begin{cases} v_d = V_{dc1}S_{dp} - V_{dc2}S_{dn} \\ v_q = V_{dc1}S_{qp} - V_{dc2}S_{qn} \end{cases} \tag{3}$$

Then (4) can be obtained

$$\begin{cases} v_d = e_d - \omega L i_q + L\dfrac{\mathrm{d}i_d}{\mathrm{d}t} \\ v_q = e_q + \omega L i_d + L\dfrac{\mathrm{d}i_q}{\mathrm{d}t} \end{cases} \tag{4}$$

PI control is adopted for the current regulator, and a voltage command is obtained as shown in (5), which is obtained from a three-level inverter using current control in two synchronous rotating dq coordinate system.

$$\begin{cases} v_d = -(K_{ip} + \dfrac{K_{ii}}{s})(i_d - i_d^*) - \omega L i_q + e_d \\ v_q = -(K_{ip} + \dfrac{K_{ii}}{s})(i_q - i_q^*) + \omega L i_d + e_q \end{cases} \tag{5}$$

Since the large coupling between the master and slave inverters, the coupling between the master inverter's own dq

axis is ignored. Considering that the current inner loop needs to obtain faster current following performance, the current loop is designed as a typical type I system, the current inner loop can be equated to an inertia link , with a time constant of inertia of $3T_s$, noted as A. On this basis, the voltage outer loop is designed, and its structure block diagram is shown in Fig. 3.

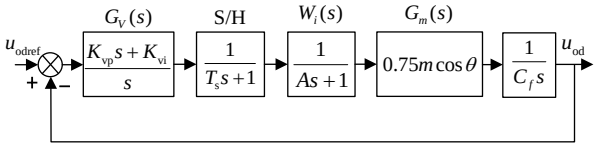

Fig. 3. Structure block diagram of voltage loop control

In Fig. 3, $G_V(s)$ denotes the voltage loop regulator transfer function, the PI regulator is used for the design of the voltage loop, K_{vp},K_{vi} are the proportional and integral coefficients respectively; S/H denotes the delay of the voltage signal sampling; $W_i(s)$ denotes the closed-loop transfer function of the current inner loop; $G_m(s)$ is the time-varying link, which is replaced by a proportional gain of 0.6; $1/C_f s$ is the transfer function of the filter capacitor. The open-loop transfer function $G_{v0}(s)$ of the system voltage loop can be obtained as shown in (6).

$$G_{v0}(s)=(K_{vp}+\frac{K_{vi}}{s})\frac{0.6}{s\bullet C_f(As+1)(T_s s+1)} \tag{6}$$

After substituting the simulated circuit parameters shown in Table I, the bode diagram of $G_{v0}(s)$ can be obtained as shown in Fig. 4.

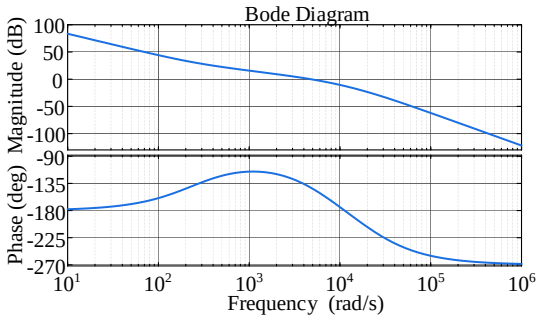

Fig. 4. Bote diagram of system open-loop transfer function

As shown in Fig. 4, the low frequency band decreases at a slope of −40dB/dec, and the high frequency band crosses the 0dB line at a slope of −20dB/dec, the crossover frequency is about 4.6kHz, harmonics and interference in the higher frequency bands can be effectively attenuated, and the phase margin is about 43°, so the system can work stably.

A current loop is adopted in the slave inverter for control. The output reference current is obtained in two parts, partly by receiving the output current of the master inverter via power/signal synchronous transmission, and partly by obtaining the current output current of the slave inverter. This reduces the coupling between the master inverter and the slave inverter, resulting in a more accurate sharing of the inverter currents.

B. Signal transmission

Binary frequency shift keying (2FSK) is one of the three common digital signal modulation methods, which uses the frequency information of the signal carrier for digital binary signal transmission. In 2FSK, the carrier frequency varies with the baseband signal between frequencies f_1 and f_2, and its expression is shown in (7).

$$e_{2FSK}(t)=\begin{cases}M\cos(\omega_1 t) & \text{Send data 1}\\ M\cos(\omega_2 t) & \text{Send data 0}\end{cases} \tag{7}$$

Based on the characteristics of the three-phase three-level inverter circuit, a composite modulation method based on the power modulation waveform can be derived, the basic principle is shown in Fig 5. Since low-frequency components are rich in the baseband signal, it is easily attenuated in the transmission process. Therefore, the baseband signal is modulated to a certain frequency band, superimposed with the power modulation waveform and sent to the SVPWM modulator for modulation. When transmitting data "1", the signal carrier frequency is f_1, and when transmitting data "0", the signal carrier frequency is f_2.

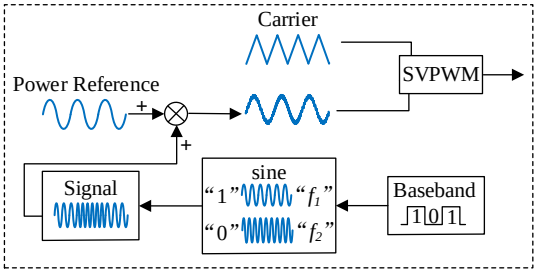

Fig. 5. Power modulation wave band modulation schematic

The output current in the rotating coordinate system on the main inverter side is converted into a 20-bit binary number, which is used as a baseband signal for modulation. The baseband signal generation process is shown in Fig. 6.

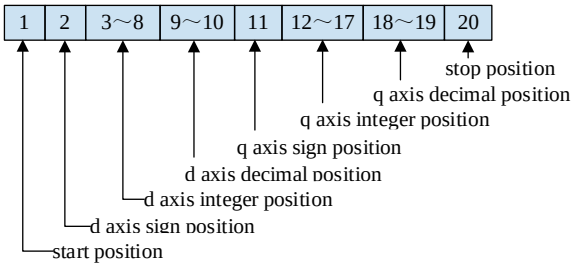

Fig. 6. Baseband signal data frame structure diagram

As shown in Fig. 6, the d-axis and q-axis can transmit integers in the range −64 to +64, with a precision of 0.25 for fractions and a demodulation error of no more than 0.125, and transmit the resulting 20-bit baseband signal at 0.005s/bit.

Non-coherent demodulation is used, whose structure mainly consists of filter, envelope detector and sampling decoder. Compared to conventional non-coherent demodulation, full-wave rectification and adders are added to the previous non-coherent demodulation. The overall demodulation strategy is shown in Fig. 7. Firstly, the load direct-axis voltage is fed into the band-pass filters with centre frequencies f_1 and f_2 respectively, and the corresponding carrier signals are demodulated. Then the waveform output from the band-pass filter is passed through a full-wave rectifier, which flips the negative half-axis portion of the waveform to the positive half-axis, and the envelope detector is performed at this point. Finally, given the adjudicator threshold, the transmitted binary data signal is demodulated,

and the resulting demodulated data signal is then converted to a decimal number, which is used as a reference for the output current from the inverter. The improved non-coherent demodulation increases the smoothness of the carrier waveform, and the problem that the three-phase wave-forms cancel each other does not exist at this point of re-summing, resulting in more complete carrier information.

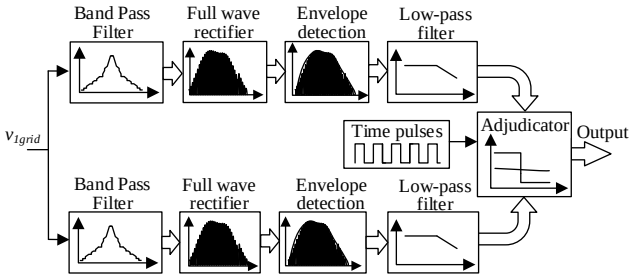

Fig. 7. Block diagram of non-coherent demodulation

Power modulated waveform frequency shift keying controls the switching circuit via a binary baseband signal, which selects two data carriers of different frequencies, resulting in a spectrum shift from baseband to frequency band signal. Since the signal is transmitted only within the set channel, the signal is less susceptible to power voltage fluctuations and has a better robustness. However, the injection of the signal changes the harmonic characteristics of the inverter output voltage. After injecting the selected 1kHz and 2kHz signals into the system, a stability analysis was carried out, and found that the selected frequencies were suitable and there were no closed-loop stability problems.

III. Simulation and Analysis

In order to verify the rationality of the above analysis and the correctness of the control strategy, the simulation platform is built and the simulation parameters are listed in Table I.

TABLE I. System Parameters

Symbol	Value	Symbol	Value
V_{dc}	1000V	f_s	20kHz
E	220V	K_{vp}	0.2
L	0.3mH	K_{vi}	50
C	20μF	A	1.5×10^{-4}
r_1	0.1Ω; 50μH	f_1 and f_2	‘0’: 1kHz ‘1’: 2kHz
r_2	0.2Ω; 100μH	A_S	1V
f	50Hz	b	200bit/s

Due to the superposition of the baseband signal, some high frequency signal ripples are generated in the obtained output voltage d-axis. The band-pass filter processed waveforms is shown in Fig. 8(b) and Fig. 8(d), where the signal wave-form is completely extracted from the power waveform with well-defined boundaries. Then the output signal is processed by the full-wave rectifier to flip the negative half-axis part of the waveform to the positive half-axis. Finally, through the upper envelope detector, the output waveforms can be obtained in Fig. 8(c) and Fig. 8(e) and then can be compared with the appropriate threshold.

The transmitted baseband signal and its corresponding demodulated signal are presented in Fig. 9. Since a certain phase lag is introduced by the bandpass filter circuit as well as the envelope detection circuit, the demodulated signal has a short delay compared to the original signal.

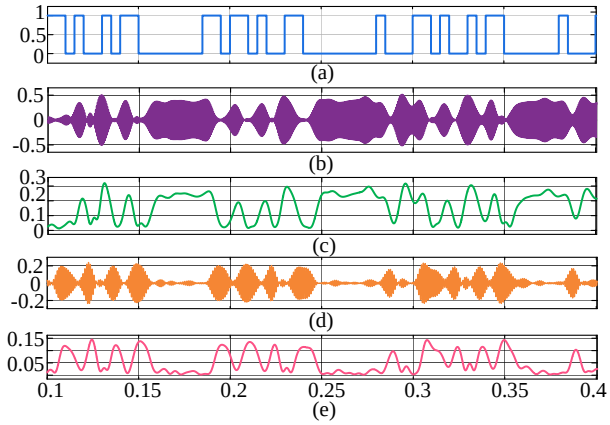

Fig. 8. Correlation waveform of power modulated waveform based signal transmission system a) baseband signal; b) "0" band signal; c) upper envelope waveform of "0" band signal; d) "1" band signal; e) upper envelope waveform of "1" band signal

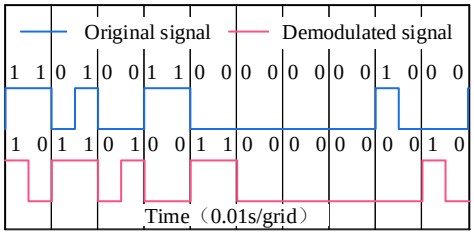

Fig. 9. The transmitted baseband signal and its corresponding demodulated signal

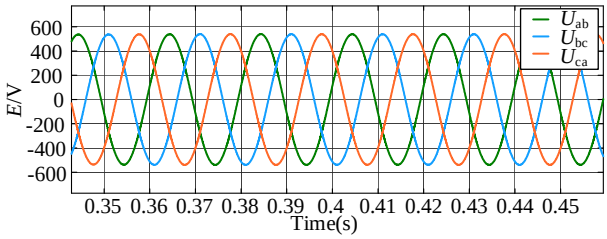

Fig. 10. Output line voltage waveform of parallel inverter

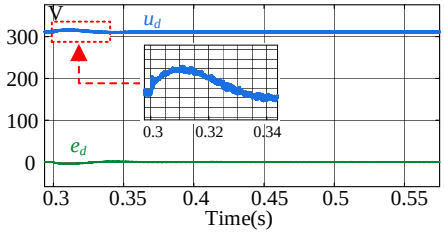

Fig. 11. Parallel inverter d-axis voltage

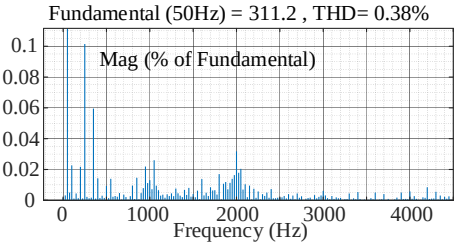

Fig. 12. System harmonic distribution

The obtained demodulated signal is inverted to decimal numbers as the reference current from the inverter. Due to the time delay of the power transfer system and the delay characteristics of the simulation module itself, the data is demodulated at 0.3s, and the reference value of the output current from the inverter is generated after arithmetic processing. The final three-phase output voltage wave-forms are presented in Fig. 10 - Fig. 12, indicating that the settling time is about 0.03s and the system harmonic component is low.

Fig. 13 shows the output currents waveforms, where ia1 is the output current of the master inverter and ia2 is the output current of the slave inverter. It can be seen that the output currents of the 2 inverters are basically the same after introducing the output current of the master inverter side at 0.3s. The difference between the steady-state output currents is tiny, which indicates the parallel inverter current sharing is realized.

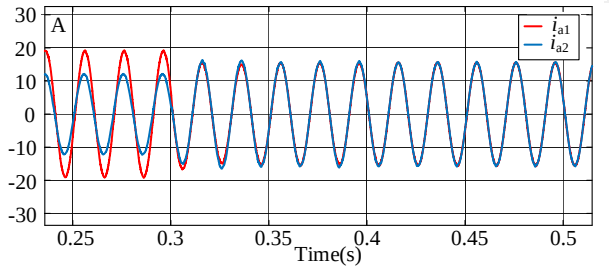

Fig. 13. Output current waveforms of parallel inverter

IV. 4 CONCLUSION

In this paper, the mathematical model of NPC three-level inverter is established and the system stability is analyzed, and a current sharing control method for parallel three-level inverters based on PSST strategy is proposed. By introducing the PSST technique on the traditional master-slave control, the information inter-action between parallel inverters is realized, then the parallel inverter current sharing is achieved, which overcome the shortcomings that the previous master-slave control requires extra communication lines for information interaction. The full-wave rectification and adder links are added on the basis of non-coherent demodulation which increases the smoothness of the carrier wave and obtains more complete carrier wave information. Furthermore, the reference current of the slave inverter is composed of the demodulated signal and its own output current to reduce the coupling between the master and slave inverter. The simulation results finally verify the effectiveness of the proposed control method.

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