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***Abstract*—Forward body biasing (FBB) is among the simplest and most effective techniques that can be leveraged to improve the performance of dynamic comparators, as previous works have demonstrated. However, none of these works puts emphasis on comparing different FBB schemes and their robustness against large differential input swings. This is especially important when considering circuits that operate at supply voltages above 0.5 V, where several approaches can be adopted for biasing the substrates without causing the body-source junctions to turn on. This paper compares three different techniques: the clocked FBB (CFBB) proposed in [1], an improvement of CFBB and a new hybrid approach that achieves the best performance in terms of delay. For the sake of brevity, the scope of our experiments has been limited to the Strong Arm latch. All simulations were carried out in a 55 nm CMOS technology at 1 V supply and 2.4 GHz clock frequency.**

***Index Terms*—Dynamic comparator, forward body biasing, strong arm latch, IoT**

I. Introduction

Due to the inherent robustness of digital circuits, modern communication systems are often designed to perform most of the processing in the digital domain. This trend, in combination with the demand for systems that are capable of handling high bit rates, makes the development of fast, power efficient mixed-signal circuits a topic of great interest.

Dynamic comparators are a key building block in most mixed-signal applications, such as analog-to-digital converters (ADC), digital-to-analog converters (DAC) and digital low drop out regulators (DLDO) and thus enhancing the figures of merit of these components is crucial for improving the performance of the systems they belong to [1]–[3].

This paper focuses on the use of forward body biasing (FBB) as a technique to reduce the delay of dynamic comparators, with minimal overhead in terms of area occupation and power consumption [4]. Implementing FBB at ultra-low supply voltages (< 0.5 V) is generally a straightforward task because the substrate terminals of the devices simply have to be tied to the supply bars (i.e. V_{dd} for the NMOS devices and ground for the PMOS devices) [5], [6]. This approach, known as swapped body biasing (SBB), becomes infeasible at medium-high supply voltages and more sophisticated approaches are required. For example, the dynamic threshold MOS (DTMOS) configurations [7], [8] or clocked FBB (CFBB) [1] can be used to avoid excessive power consumption and minimize the risk of latch-up. This is especially important in dynamic comparators, where output and internal nodes experience voltage variations across the full available swing (from V_{dd} to GND). Although previous works have explored the use of FBB in dynamic comparators, none of them has thoroughly discussed and compared different approaches and their tradeoffs.

This paper provides the following contributions. First of all, we discuss the advantages and the limitations that characterize FBB in dynamic comparators at medium-high supply voltages. Then, we show that the CFBB technique proposed in [1] suffers from robustness issues when large input differential voltages are applied to the comparator, and we provide an interpretation for this phenomenon. Based on our analysis, we propose two alternative approaches: a simple improvement of the original CFBB and a new hybrid FBB (HFBB) scheme that exploits diode-connected transistors to bias the substrate terminals of the PMOS devices. Finally, we compare the simulated performance of the three FBB techniques (CFBB, improved CFBB, and HFBB) at 1 V supply and show that the proposed HFBB scheme achieves the smallest delay and power-delay-product (PDP).

The paper is organized as follows: section II discusses from a theoretical standpoint the advantages and the limitations of FBB in dynamic comparators at medium-high supply voltages. Section III analyzes the robustness issues that affect the CFBB Strong Arm from [1] and describes the improved CFBB and the HFBB techniques. Section IV compares the simulated performance of the three FBB schemes. Section V concludes the paper.

II. Characteristics and requirements of FBB schemes

Figure 1 shows the Strong Arm latch. The circuit consists of a clocked differential pair loaded by two cross-coupled inverters that regenerate the input difference during the evaluation phase. Four clocked PMOS devices are used to precharge nodes P, Q, X and Y during the reset phase, so as to cancel the effect of the previous decision. For the sake of generality, the voltages of the substrate terminals of M3-M4-M5-M6 have been left unspecified. Clearly, in the conventional topology one has $V_{b3} = V_{b4} = 0$ V and $V_{b5} = V_{b6} = V_{dd}$.

According to [9], the time needed by the comparator to reach an output differential voltage ΔV_{od} given an input difference V_{id} can be expressed analytically as

$$t_d = \frac{C_L V_{th5,6}}{I_{tail}} + \frac{C_L}{g_{m,eff}} \ln\left\{ \frac{1}{V_{th5,6}} \sqrt{\frac{I_{tail}}{2\beta}} \frac{\Delta V_{od}}{V_{id}} \right\} \quad (1)$$

where β is the transconductance coefficient, $V_{th5,6}$ are the threshold voltages of M5-M6, C_L is the load capacitance,

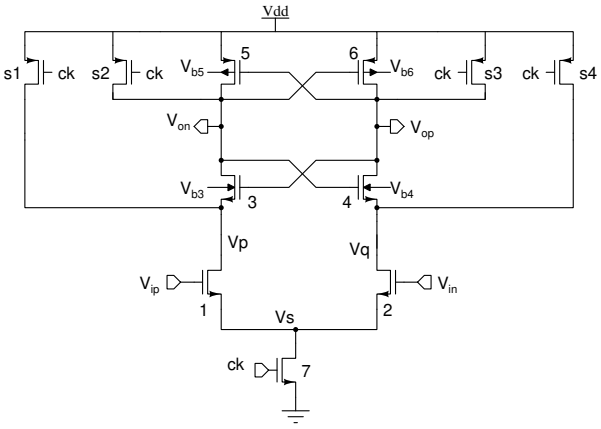

Fig. 1: Strong Arm latch.

I_{tail} is the tail current (which we approximate as constant) and $g_{m,eff} := g_{m3,4} + g_{m5,6}$. Note that $\tau_{reg} := C_L/g_{m,eff}$ is the comparator's regeneration time constant. Equation 1 shows that applying FBB to M3-M4-M5-M6 can be expected to improve the delay because it reduces $V_{th5,6}$ and therefore the first term in equation 1 becomes smaller. In addition, the transconductance of M3-M4-M5-M6 (and, therefore, $g_{m,eff}$) increases.

At medium-high supply voltages, FBB must be implemented carefully to prevent the body-source junctions from turning on, as this would increase the power consumption and the risk of latch-up. For this reason, the V_{bs} of the NMOS devices and the V_{sb} of the PMOS devices should remain well below 0.6 V during operation.

Ideally, an FBB scheme should satisfy the following requirements:

1) The designer should be able to apply FBB to all the relevant devices to maximize the improvement in terms of delay.
2) It should ensure that the body-source voltages stay limited during operation.

In the next sections we explain how the CFBB technique from [1] fails at satisfying these two requirements and we propose two different FBB schemes that improve on these aspects.

III. FBB SCHEMES FOR THE STRONG ARM LATCH

Figure 2a shows the CFBB scheme proposed in [1]. In order to illustrate the working principle of this FBB scheme we will refer to the model in Figure 3, where M8 is modeled as a switch with a parallel parasitic capacitance. The gate-body equivalent capacitances are not shown because they end up in parallel to the body-drain capacitances.

- *Reset Phase:* during the reset phase M8 pulls $V_{b3,4}$ to V_{dd}. Since $V_p = V_q = V_{op} = V_{on} = V_{dd}$ the total charge at node B is 0.
- *Evaluation Phase:* during the evaluation phase M8 turns off, leaving node B floating. For the sake of simplicity we will assume that this happens before V_p and V_q start to drop. As voltages V_p, V_q, V_{op} and V_{on} change, charge redistribution occurs at node B and $V_{b3,4}$ changes according to the following equation:

$$V_{b3,4} = \frac{C_{bd}(V_{on} + V_{op}) + C_{bs}(V_p + V_q) + C_8 V_{dd}}{2C_{bd} + 2C_{bs} + C_8} \quad (2)$$

This way, the comparator's regeneration time is reduced because $V_{b3,4}$ will settle at a voltage $0 < \bar{V} < V_{dd}$

Equation 2 shows that $\bar{V}$ can be tuned by acting on C_8 (that is, on M8's area).

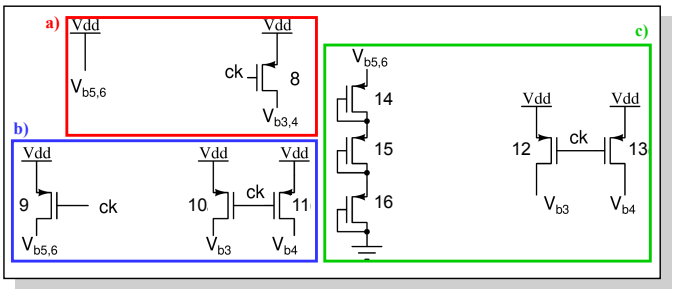

Fig. 2: FBB schemes for the Strong Arm latch: a) CFBB from [1], b) improved CFBB and c) HFBB.

The CFBB scheme we just described exhibits two significant limitations. Firstly, FBB is not fully exploited because the substrate terminals of M5-M6 are not biased. Secondly, large differential input voltages cause a substantial increase in V_{bs}. When V_{id} is low, both V_p and V_q are rapidly discharged to GND, and according to equation 2, $V_{b3,4}$ settles at $\bar{V}_b = V_{dd}(C_{bd} + C_8)/(2C_{bd} + 2C_{bs} + C_8)$. However, when V_{id} is high, one of the input devices (M1-M2) may be partially or completely off, resulting in incomplete discharge of either V_p or V_q. For instance, if $V_{id} = V_{dd}$, then V_q remains charged at $\approx V_{dd}$. Consequently, $V_{b3,4}$ settles at $V_{dd}(C_{bs} + C_{bd} + C_8)/(2C_{bd} + 2C_{bs} + C_8) > \bar{V}_b$. As we will show in the next section, in such cases $V_{bs_{3,4}}$ may easily exceed 0.6 V, which is not acceptable for safe operation.

To address these limitations we devised an improved CFBB scheme, which is depicted in figure 2b. In this revised scheme, M8 is replaced by two distinct devices. By avoiding to short-circuit the substrate terminals, excessive increases in the devices' V_{bs} are prevented, as charge redistribution can occur independently at the two nodes. Indeed, one has

$$V_{b3} = \frac{C_{bd}V_{on} + C_{bg}V_{op} + C_{bs}V_p + C_8 V_{dd}}{C_{bd} + C_{bg} + C_{bs} + C_8} \quad (3)$$

which entails that V_{b3} only depends on V_p. In this case, the gate-body equivalent capacitance does not end up in parallel to the C_{bd} so it must be made explicit. Similar considerations hold for V_{b4}. Furthermore, another device is added so that FBB can be applied to M5-M6 as well. The substrate terminals of M5-M6 can be tied together because the common-mode swing at the output terminals barely depends on the input difference and their source terminals are always at V_{dd}. The main drawback of this design is that V_{sb5} and V_{sb6} remain exiguous ($\approx 0.2V$) because the output common mode only decreases by $\approx V_{dd}/2$ during evaluation. This limits the

improvement in delay. It should be noted that a clocked NMOS device cannot be used to bias the body terminals of M5-M6 because $V_{sb5,6}$ would be equal to V_{dd} during the reset phase.

To achieve a further improvement in comparison speed we propose a new hybrid FBB (HFBB) scheme, which is shown in Figure 2c. In this topology, three series-connected diodes (implemented with PMOS devices) generate the bias voltage for the substrate terminals of M5-M6. Therefore, the value of V_{bp} results from a nonlinear resistive divider. From a practical point of view, V_{bp} can be adjusted by acting on the number of stacked diodes and/or on their aspect ratios. As in the improved CFBB, the substrate terminals of M5-M6 can be tied together because the signal swings at the output nodes are independent of V_{id}. Transistors M3-M4, instead, are biased with the previously described CFBB scheme. As we will show

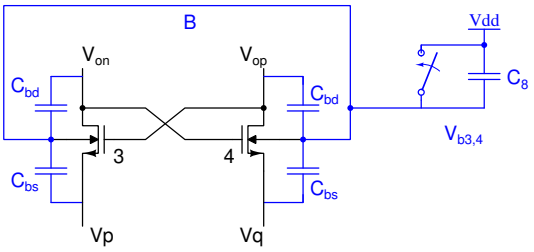

Fig. 3: Charge redistribution model for the CFBB circuit.

in the next section, this scheme achieves the best performance in terms of delay, because $V_{sb5,6}$ can be set between 0.4 V and 0.5 V. Furthermore, the enhanced CFBB scheme addresses the robustness issues that can arise when large differential signals are applied to the input.

IV. Comparison

The three FBB-based topologies from the previous section and the conventional Strong Arm latch have been designed and simulated in a commercial 55 nm CMOS technology at 1 V supply. All the delay and power consumption values reported in this section have been evaluated at an input differential voltage of 1 mV and a clock frequency of 2.4 GHz. Table I

TABLE I: Sizing of the devices shown in Figures 1 and 2. All devices have minimum channel length ($L = 0.60$ µm).

Device	7	1-2	3-6	8	9	10-13	14-16	$s1$-4
W [µm]	16.0	8.0	2.0	2.0	0.135	0.4	0.135	0.5

shows the sizing of used for the Strong Arm comparator and the body biasing circuits. To ensure a fair comparison a unique sizing was adopted for the comparator core, while the devices used for implementing FBB were optimized independently. It is worth noticing that the impact of such devices on area is negligible because they have minimum or near-minimum channel width.

Figure 4 shows the transient behaviour of the output voltages in the conventional Strong Arm latch and in the three FBB-enhanced versions (CFBB, improved CFBB and hybrid FBB). The improved CFBB and the hybrid FBB clearly achieve better regeneration times with respect to the original CFBB. The hybrid FBB, specifically, achieves the best delay among the three schemes.

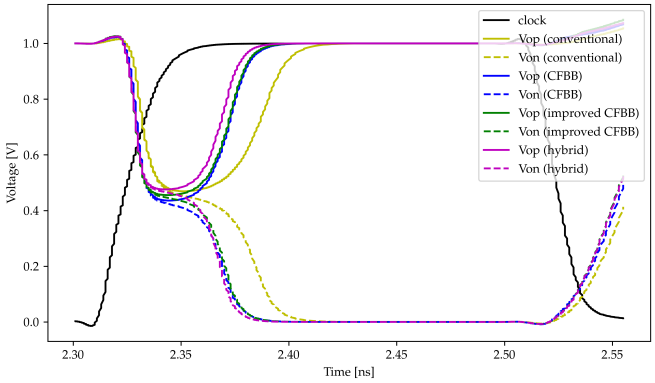

Fig. 4: Simulated transient behaviour of the output voltages in the different FBB schemes with $V_{id} = 1$ mV.

Figure 5a compares the transient behaviour of the body-source voltages in the three FBB schemes when $|V_{id}| = 1$ mV. At the first cycle, an input differential voltage $V_{id} = 1$ mV is applied; then, at the subsequent cycle, the sign of V_{id} toggles, so the input becomes -1 mV. The figure shows that the body-source voltages stay well below 0.6 V, except for the reset phase, during which the V_{bs} of the NMOS devices rises above 0.6 V. However, during this phase no static current can flow through the source terminals of M3-M4 (because M9 is in off state) so there is no risk of latch-up, nor any increase in power consumption. Figure 5b, instead, shows the transient behaviour of the body-source voltages with $V_{id} = 500$ mV (first clock cycle) and V_{id} = -500 mV (second clock cycle). In the topology from [1] V_{bs3} rises above 0.6 V because only one of V_p and V_q gets discharged. On the other hand, V_{bs3} and V_{sb5} remain below 0.6 V by a wide margin in the CFBB and the hybrid FBB schemes.

Table II compares the simulated performance of the CFBB scheme from [1], the improved CFBB scheme and the new HFBB scheme, respectively. $V_{bs,n}^{max}$ and $V_{sb,p}^{max}$ represent the

TABLE II: Comparison between the simulated performance of conventional, CFBB, improved CFBB and HFBB Strong Arm.

	Conventional	CFBB	improved CFBB	HFBB
P [µW]	90.6	90.2	89.5	92.2
t_d [ps]	63.2	57.7	56.4	52.8
PDP [fJ/conv.]	5.73	5.20	5.05	4.87
EDP [fJ/(GHz)]	2.38	2.16	2.10	2.03
$V_{bs,n}^{max}$ [mV]	-	474	476	473
$V_{sb,p}^{max}$ [mV]	-	-	204	467

maximum body-source (source-body) voltages of the NMOS (PMOS) devices during the evaluation phase. The reduction in delay is quite limited in the improved CFBB Strong Arm, because body biasing on the PMOS devices is not sufficient. The hybrid FBB Strong Arm achieves the best performance in terms of delay thanks to the diode-based biasing. Hybrid FBB also shows the highest power consumption because leakage currents become larger; however the proposed approach is still

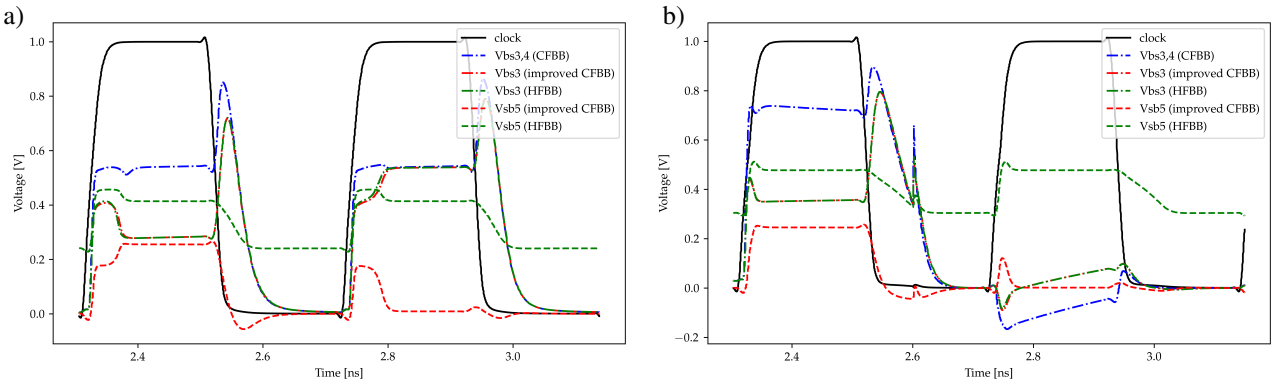

Fig. 5: Transient behaviour of the body-source voltages for the different FBB schemes with $|V_{id}| = 1$ mV a) and $|V_{id}| = 500$ mV b).

advantageous because of the strong improvement in delay. This is confirmed by the fact that the circuit exhibits the lowest PDP.

Table III shows the performance of the proposed hybrid FBB scheme under process, temperature and voltage variations. The circuit shows good robustness under a wide range of operating conditions, with body-source voltages remaining below 0.6 V by a large margin. Though not shown in the table, our simulations demonstrated that the advantage that HFBB has over the conventional and CFBB schemes remains fairly consistent in all corners. Finally, in Tab. IV a comparison with high-speed Strong Arm-based comparator from state-of-the-art literature has been reported. As it can be observed, the HFBB architecture reaches the lowest delay whereas the smallest EDP is achieved by [1].

TABLE III: Performance of the Strong Arm comparator with the proposed HFBB scheme under PVT variations, with $V_{dd}^{min} = V_{dd} - 5\%V_{dd}$, $V_{dd}^{max} = V_{dd} + 5\%V_{dd}$, $T^{min} = 0$ °C and $T_{max} = 80$ °C.

	V_{dd}^{min}	V_{dd}^{max}	T^{min}	T^{max}	FF	SS	FS	SF
P [µW]	81.3	104	88.6	99.4	96.5	91.4	92.8	93.0
t_d [ps]	57.9	48.8	52.3	54.4	48.1	55.1	47.9	56.3
PDP [fJ/conv.]	4.71	5.07	4.63	5.40	4.64	5.04	4.45	5.24
EDP [fJ/(GHz)]	1.96	2.11	1.93	2.25	1.93	2.10	1.85	2.18
V_{bsn}^{max} [mV]	451	495	470	483	518	463	493	467
V_{sbp}^{max} [mV]	456	478	470	422	439	487	443	491

TABLE IV: Comparison between recent literature and the topologies that have been simulated in this work.

	This Work				Literature		
	HFBB	Improved CFBB	CFBB	Conv.	[1]	[2]	[3]
Year	2023	2023	2023	2023	2018	2020	2020
Technology [nm]	55	55	55	55	65	90	65
V_{dd} [V]	1	1	1	1	1	1.2	1
V_{id} [mV]	1	1	1	1	1	20	2
t_d [ps]	52.8	56.4	57.7	63.3	237	80	167
Energy/comp. [fJ]	38.4	37.3	37.6	37.8	3.91	32.8	108
EDP [fJ/(GHz)]	2.03	2.10	2.16	2.38	0.926	2.62	18.0

V. Conclusions

This paper provided a comprehensive analysis of three different FBB techniques. Specifically, we discussed and compared the performance of three different body-biasing schemes: the CFBB technique from [1], a simple improvement of this technique, and a hybrid scheme that combines the improved CFBB with a new diode-based approach. The improved CFBB scheme ensures that the body-source voltages of the NMOS devices remain well below 0.6 V even when large differential inputs are applied to the comparator, which is not true for the original CFBB. However, there is a limited reduction in delay because the substrates of M5-M6 are not biased properly. The hybrid FBB scheme solves this issue by using series-connected diodes to generate the bias voltage for the PMOS devices. Thanks to this technique, the hybrid FBB Strong Arm achieves the best delay among the three versions, with a 16.5% improvement with respect to the conventional Strong Arm and a 8.4% improvement with respect to the CFBB-based Strong Arm.

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