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December 25, 2019

Variability Analysis of On-chip Graphene Interconnects at Subthreshold Regime

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Abstract: In today's modern era, zest for low power applications and miniaturized gadgets has increased tremendously. Operating devices and circuits in subthreshold region of operation is an optimum technique to attain low power requirements in the system. On-chip interconnects that connect and facilitate signal transmission between devices and different modules as well as provide power and clock connections are one of the dominating parts of system. At deep submicron technologies, interconnects majorly affect and are deciding output performance parameter. To get higher performance, copper on-chip interconnects have been replaced by next-generation graphene interconnects. At miniaturized technology nodes, variation due to temperature, fabrication process and environmental fluctuations crops up significantly that varies the system output in on-chip ICs. As a result, variability analysis of on-chip interconnects at nano regime in subthreshold region has become need of the hour. In the present paper, effective variability analysis of graphene interconnect in subthreshold region is presented for the first time to the best of the knowledge of authors. Process corner, parametric and Monte-Carlo analyses have been performed to determine variability effect in on-chip multilayer graphene nanoribbon (MLGNR) interconnects. The different variability analyses have been performed at 32nm technology node.

Keywords—Integrated circuit, Interconnect, Propagation delay, Subthreshold region, Variability, VLSI

I. INTRODUCTION

The term variability refers to the fluctuation in parameters under consideration. At nano-dimensions, variation due to process, voltage and temperature results in fluctuation of output system performance [1]. These variations happen because of fluctuation in parameters at designing, fabrication and manufacturing levels. Parameter variation causes degradation in overall circuit performance. Circuit performance becomes unpredictable due to less control over physical parameters at manufacturing process level. As device density reduces, circuit becomes more sensitive towards the process variations. Parameter variations increase at miniaturized technology nodes and cause various system integrity issues [2]. As circuit designer, these impact of parameters need to be taken into account to improve performance and reliability [3]. Assessing the effect of various parameter variations can be effectively performed using variability analysis.

Variation can be broadly classified into two types viz. process and environmental. Process variations refer to fluctuation from die to die or within die while environmental variations can be due to external sources such as temperature or voltage fluctuation [1]. Inter-die variations constitute dominant factor in determining circuit output performance. As die-size increases, intra-die variation becomes more dominant [3]. Intra-die variation occurs within die and generally increases due to manufacturing defects. Intra-die variation can be broadly classified in three types as: device variation, interconnect variation and dynamic variation. Device variation includes fluctuation in device related parameters such as effective gate length, threshold voltage and oxide thickness. These variations occur at different fabrication steps such as patterning, etching and deposition. Interconnect variation includes fluctuation in width, spacing, thickness and height of interconnect. Dynamic variations include fluctuation due to external sources such as voltage and temperature [4-5].

In VLSI, millions of transistors are integrated on a single chip. The transistors are connected with each other by on-chip interconnects. These interconnects also provide power and ground signals to devices. At higher technology nodes, devices are dominant in determining system performance. However, at lower technology nodes, interconnect becomes more significant than transistors. Interconnect affects the overall system efficiency and degrades system performance. This also causes delay, power dissipation and crosstalk in ICs [6].

The ITRS reports also indicate the significant deviation effects due to variability in interconnect parameters [7-8]. Variability analysis in subthreshold region of operation of devices and interconnects has been performed in [7]. Variability analysis of subthreshold source coupled logic circuits is performed in [8]. They have shown that the source coupled logic is very impactful against both on-chip variations in die-to-die and within die.

For on-chip interconnects, copper is one of the aptly suited and widely used material for interconnects. But as device dimensions scale down in nano regime, copper has become absolute because of varying non-ideal effects which get aggregated at lower dimensions. To mitigate this issue, carbon based graphene has been investigated as the potential interconnect material and is suitable to replace copper due to its magnificent magnetic and electrical properties [6, 9]. Graphene based interconnect can be of different structures as carbon nanotube and graphene nanoribbon. Amongst different forms of graphene structures, multi-layer graphene nano-ribbon (MLGNR) has become optimum choice for on-chip

interconnects due to its higher performance such as lower delay, power dissipation, limited crosstalk effect and also due to fabrication feasibility [10-12].

Variability analysis in graphene interconnects have also been investigated by many researchers [3,13-17]. Temperature, contact resistance and metallic ratio are the process dependent parameters. These parameter for CNT bundle interconnect has been broadly analyzed in [3]. The design and manufacturing challenge along with variability issues in copper and graphene interconnect have been performed in [13-15]. Impact of variability on SWCNTs bundles and MWCNT interconnects have been given in [16]. The authors compared the performance of SWCNT bundle and MWCNT interconnects under process effects. An effective process induced variation effect on MLGNR has been shown in [17]. It is analyzed that average deviation in delay is nominal for different process induced parametric variations.

For low power applications especially in small and portable e-gadgets, voltage scaling is one of the optimum suited techniques [18]. Low voltage operation of devices and interconnects can be effectively modeled in subthreshold region. With increasing demand of low power portable and e-systems, subthreshold region of operation has become widely popular. Analysis of copper interconnect in subthreshold region has been presented in [18]. Analytical models for copper interconnects in subthreshold region of operation have been formulated in [19]. Subthreshold region of operation in advanced nano-materials like CNTs and GNRs is new exciting and challenging topic of research. The variability analysis of next-generation graphene interconnects operating in subthreshold region is a major concern and has not been taken up yet to the best of our knowledge. Hence, encouragingly, this has been novelly taken up in the present research work to effectively analyze and study the paradigm of variability effects in graphene interconnects in subthreshold region.

The paper comprises of five sections. This section gives the introduction of the paper. Next section details about subthreshold region of operation. Formulations for parasitic extraction of MLGNR interconnect are stated in section 3. Section 4 describes the several variability analyses considered in the paper as well as the corresponding results. Section 5 is the conclusion.

II. SUBTHRESHOLD REGION OF OPERATION

During subthreshold region of operation, gate to source voltage (V_{gs}) is lower or equivalent to threshold voltage (V_{th}) of MOSFET i.e. $V_{gs} \leq V_{th}$ [18-20]. Minority carriers are present in gate when $V_{gs} \leq V_{th}$. Due to these carriers, small amount of current will flow through the circuit. These low minority carrier injections from source to drain and henceforth low current flow within the device can be used for implementing several low power logic circuit analysis.

The current in subthreshold region of operation is given as:

$$I_D = \frac{\mu_n C_{OX} W}{L_{eff}} (\eta - 1) V_T^2 e^{\frac{V_{gs}-V_{th}}{nV_T}} \left(1 - e^{-V_{ds}/V_T}\right) \quad (1)$$

where, V_{ds} is the drain to source voltage, W and L_{eff} are channel width and effective gate length of MOSFET respectively, C_{OX} is the oxide capacitance, μ_n is the mobility, V_T is thermal voltage and η is slope factor and is defined as:

$$\eta = 1 + \frac{C_D}{C_{OX}} \quad (2)$$

where, C_D is depletion layer capacitance.

III. FORMULATIONS FOR PARASITICS DETERMINATION OF MLGNR INTERCONNECT

The formulation for determining parasitic elements of MLGNR interconnect are detailed in this section.

The resistance (R_{GNR}) of MLGNR interconnect is expressed as [21] :

$$R_{GNR} = \frac{\hbar/2e^2}{N_{ch} N_{layer}} \quad (3)$$

where N_{ch} is the number of conducting channels (modes) in one layer, N_{layer} is the number of GNR layers. $\hbar$ is Planck's constant and e is electronic charge.

In MLGNR interconnect, there exists two types of inductance viz. magnetic (L_M) and kinetic (L_K). These are obtained as [12]:

$$L_M = \frac{\mu d}{w} \quad (4)$$

$$L_k = \frac{(\hbar/4e^2)\, v_f}{N_{ch} N_{layer}} \quad (5)$$

where, v_f is the Fermi velocity, d is diameter of interconnect, w is the width of interconnect and μ is permeability.

The MLGNR comprises of electrostatic (C_E) and quantum (C_Q) capacitances. These are given as [21]:

$$C_E = \frac{\varepsilon w}{d} \quad (6)$$

$$C_Q = N_{ch} N_{layer} \frac{4e^2}{\hbar v_f} \quad (7)$$

where, ε is permittivity.

The equivalent inductance and capacitance of MLGNR interconnects are defined as:

$$L_{GNR} = L_M + L_K, \; C_{GNR} = \frac{C_E C_Q}{C_E + C_Q} \quad (8)$$

IV. VARIABILITY ANALYSIS OF MLGNR INTERCONNECTS IN SUBTHRESHOLD REGIME

In this section, a variability effect in graphene based MLGNR interconnects in subthreshold region of operation is presented. For effective analysis, a comparison of MLGNR with traditional copper interconnect has also been made. For the several variability analyses performed, the technology node considered is 32nm [22]. The driver-interconnect-load (DIL) model is used for the analysis [23]. This is shown in Fig. 1. V_{in} is the input pulse signal with signal transition period of $1ns$ and pulse period of $1us$. Major challenge in subthreshold circuit designing is its very high sensitivity to process, voltage and temperature variations. This is due to the fact that current in subthreshold region is defined by exponential function that results in large deviation in output current due to small variation in any of the input parameters [24-26]. Three of the important variability analyses that have been conducted and presented in this paper are process

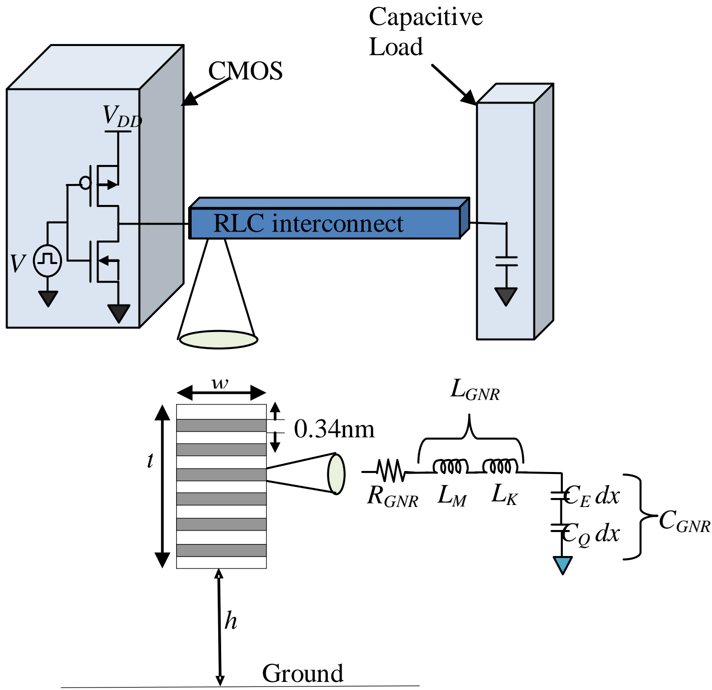

Fig. 1. Driver-interconnect-load (DIL) model.

corner, parametric and Monte-Carlo. The effects of different varying parameters viz threshold voltage (V_{th}), effective gate length (L_{eff}), oxide thickness (T_{ox}), and supply voltage (V_{DD}) have been considered.

A. *Process corner analysis*

Process corner analysis determines the circuit performance at different technology process corners. Due to several non-ideal fluctuations that occur during fabrication processes, several parameter of the device varies. The developed devices from the same fabrication lot show different electric characteristics. Depending on varying characteristics, these devices are categorized as different process model files and are often referred as process corner files. The different process corners considered are Fast NMOS-Fast PMOS (FF), Slow NMOS-Slow PMOS (SS), Slow NMOS-Fast PMOS (SF), Fast NMOS-Slow PMOS (FS) and Typical NMOS-Typical PMOS (TT). Process corner analysis helps to assess the circuit performance at worst possible conditions [1, 4, 5, 8]. In the present work, power dissipation and delay are computed at different process corners.

Power and delay are analyzed with varying temperature. Temperature is varied from -25°C to 100°C. Power dissipation and delay are computed as ratio of MLGNR to copper interconnects. If the value of this ratio is unity, then this signifies that both the copper and MLGNR interconnects have comparable performance. If MLGNR to copper ratio is higher than unity, it reflects that copper interconnect possess better performance than its counterpart MLGNR interconnect. However, in the other case (i.e. ratio lesser than unity) indicates that performance of MLGNR interconnect is superior than copper interconnect. From Figs. 2 and 3, it can be seen that the ratio of MLGNR to copper interconnect for both power dissipation and delay are lesser than unity. This convincely reflects that MLGNR interconnects possess higher performance. In Fig. 2, it is seen that power ratio increases marginally with temperature. It is also analyzed that FF process corner model possesses the highest power dissipation while SS model has least power dissipation. Fig. 3 gives delay variation with temperature at different process corners. Since FF corner model has attribute of fast operation, it results in lower delay in circuit and same can be seen in Fig. 3.

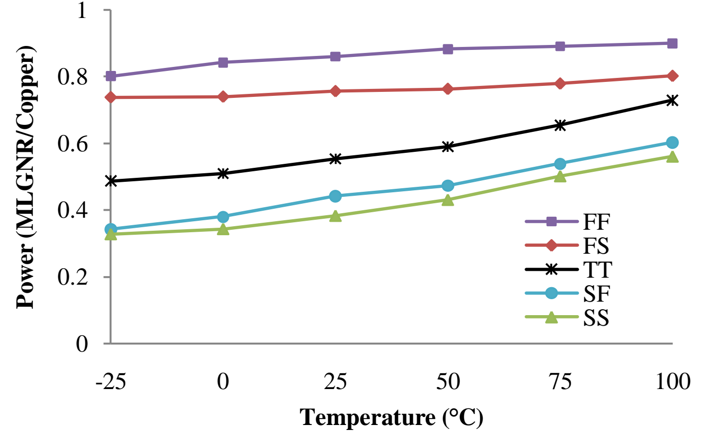

Fig. 2. Power dissipation analysis of graphene and copper interconnects with respect to temperature.

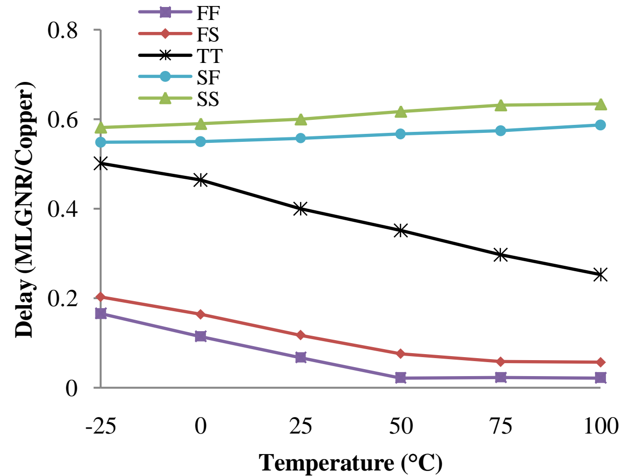

Fig. 3. Delay analysis of graphene and copper interconnects with respect to temperature.

a) *Parametric sensitivity analysis*

Parametric sensitivity analysis deals with the variation of single parameter at a time. The considered parameters for analysis are threshold voltage (V_{th}), effective gate length (L_{eff}), oxide thickness (T_{ox}) and supply voltage (V_{DD}). In this analysis, power dissipation and delay are computed by varying each of these parameters one at a time.

(i) Threshold voltage (V_{th})

Threshold voltage variations occur due to dopant variations at the fabrication level [27]. The parameters are varied by ±3σ, where σ is the standard deviation for the Gaussian distribution function. The standard deviation for threshold voltage is taken as 12.5% [28]. The nominal value of threshold voltage at 32nm technology node of NMOS

transistor is 0.3V. Power dissipation and delay are analyzed for copper and graphene interconnects as shown in Fig. 4.

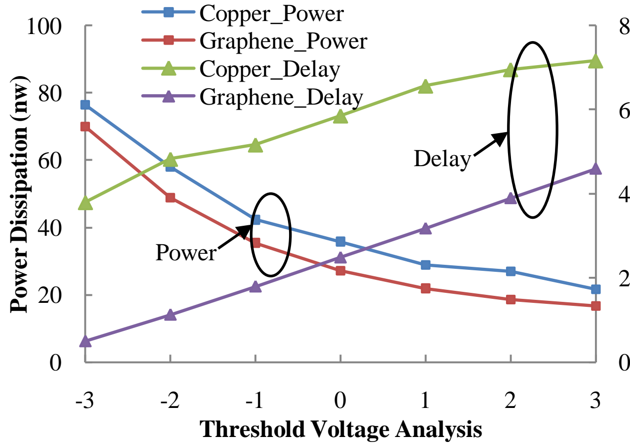

Fig. 4. Power dissipation and delay analyses of interconnects by varying threshold voltage.

From Fig. 4, it is seen that delay increases with increase in threshold voltage value. This is because as threshold value increases the device switching time increases. Consequently, device becomes slow. This is also evident from MOS drain current equation for subthreshold region as stated in (1).

From equation (1), it can be inferred that

$$I_D \propto e^{(V_{gs}-V_{th})} \quad (9)$$

Henceforth, for constant V_{gs} value, increase in threshold voltage value results in decrease in drain current. Consequently, delay in interconnect system goes on increasing with increase in threshold voltage. However trend of power dissipation is opposite to that of delay. For example, with increase in threshold voltage from 0.33V (-3σ) to 0.36V (+3σ), power dissipation in graphene interconnect decreases from 70nw to 16.7nw and for copper interconnect, power dissipation decreases from 76.5nw to 21.6nw. It can be also analyzed from Fig. 4 that graphene interconnect gives higher performance in terms of both lower delay and power dissipation than copper interconnects.

(ii) Oxide thickness (T_{ox})

Oxide thickness variation generally occurs during device deposition and masking processes [29]. The ±3σ percentage variation in oxide thickness has been taken as 4% [28]. The nominal, minimum and maximum values of oxide thickness considered corresponding ±3σ deviation are 1.65nm, 1.584nm and 1.71nm respectively. The variability effect due to oxide thickness variation is illustrated in Fig. 5. It is analyzed that as oxide thickness increases, delay decreases while power dissipation increases. For example increase in oxide thickness from 1.65nm to 1.71nm results in 10.26% decrease in delay. For the same variation in oxide thickness, power dissipation increases by 20%.

(i) Effective gate length (L_{eff})

Channel gate length variation occurs due to irregularities in lithography process. This results in various short channel effects in the devices [24-25]. The variation in gate length is taken as ±15% [28]. Power dissipation and delay are analyzed for copper and graphene interconnects by varying gate length. This is shown in Fig. 6.

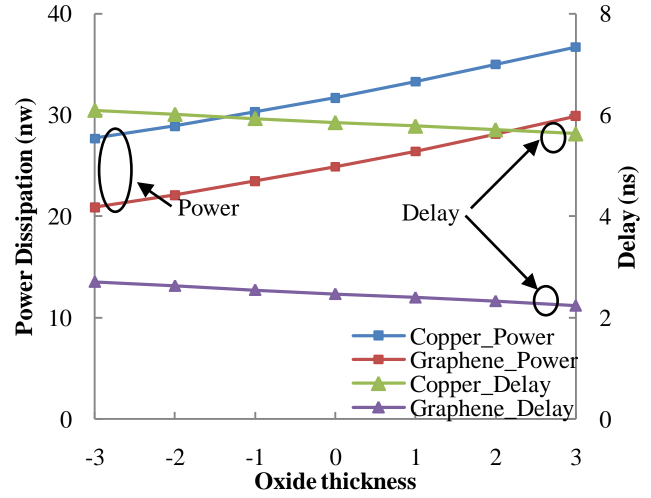

Fig. 5. Power dissipation and delay analyses of interconnects by varying oxide thickness.

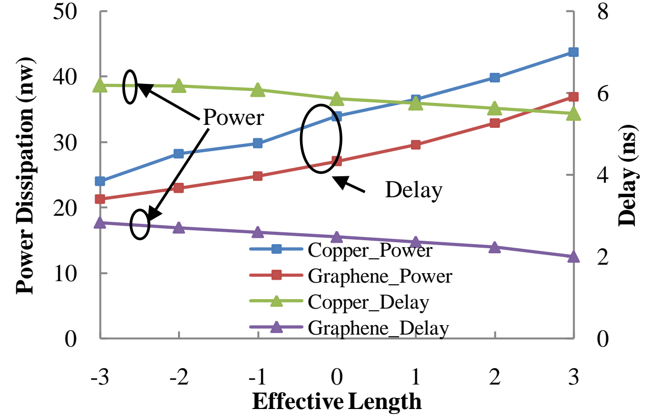

Fig. 6. Power dissipation and delay analyses of interconnects by varying effective gate length.

From equation (1), it can be deduced that,

$$I_D \propto \frac{1}{L_{eff}} \quad (12)$$

Hence, reduction in gate length leads to higher current. Higher current consequently leads to faster operation of device and system. This can be seen from Fig. 6. that as gate length increases, delay increases and power dissipation decreases.

It is also computed from figure that delay variation for graphene interconnect at ±2σ is 2.8ns and 2ns. The variation in copper interconnect is 6.3ns and 5.8ns at ±2σ.

(ii) Supply Voltage Variation (V_{DD})

Supply voltage variation can occur due to packaging irregularities and power fluctuations.

For voltage variability analysis, V_{DD} is varied by ±10% [28]. Voltage fluctuation causes switching voltage variation at the output node that result in fluctuation of the output parameter. The interconnect can be modeled as inductance,

capacitance and resistance. As supply voltage changes, current changes and correspondingly voltage drop across these parasitic elements of interconnect also changes. These overall affects the system performance [1]. In Fig. 7, variation in power dissipation and delay are shown for copper and graphene interconnects by varying supply voltage.

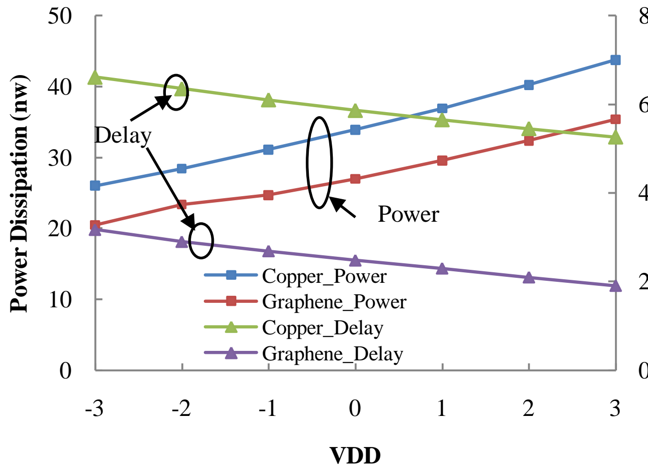

Fig. 7. Power dissipation and delay analyses of interconnects by varying supply voltage.

From Fig 7, it is seen that power dissipation increases with increase in supply voltage. This is evident as higher supply voltage results in higher current through the device and interconnects. This correspondingly results in more IV losses in the system. It is analyzed that power dissipation increases by 1.31 and 1.28 times as supply voltage change from 0.501V to 0.551V for graphene and copper interconnects respectively.

(iii) Interconnect variation

Due to process and fabrication non uniformities, variations also occur in interconnect structures. For example, during photo lithography and etching processes, interconnect width and spacing varies. Intra-layer thickness and height varies due to deposition and chemical mechanical polishing (CMP) processes [27]. The interconnect parameters considered for the variability analysis are

(a) Interconnect width (W_i),
(b) Spacing between two interconnects (S_i),
(c) Height of interconnect from the substrate (H_i)
(d) Thickness of dielectric (T_i).

Parameters (nm)	Nominal value	Minimum value	Maximum value
Width (W_i)	250	225	275
Spacing (S_i)	250	225	275
Height (H_i)	585	526.5	643.5
Thickness (T_i)	375	337.5	412.5

The interconnect parameters are varied as ±10% [28]. Power dissipation and delay for copper and graphene with varying interconnect parameters are shown in Fig. 8. From the figure, it is analyzed that variability effects in both copper and graphene structure are quite nominal for all the deviations of interconnect parameter.

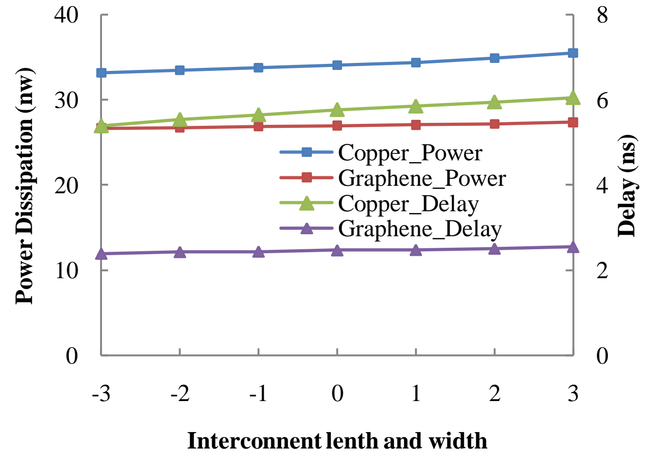

Fig. 8. Power dissipation and delay analyse with interconnect parameter variation.

C) Monte-Carlo analysis

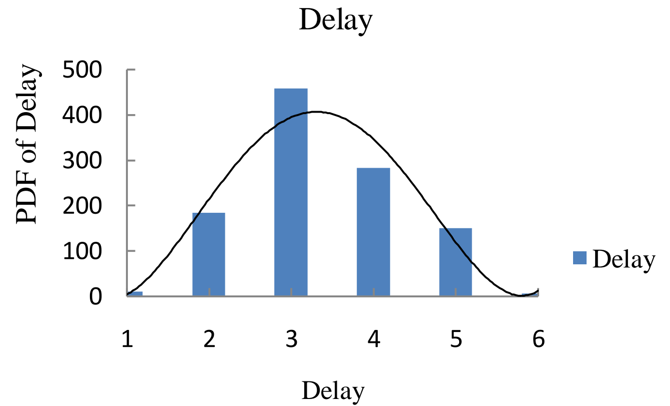

Fig. 9. Probability distribution function for delay obtained using Monte-Carlo simulation.

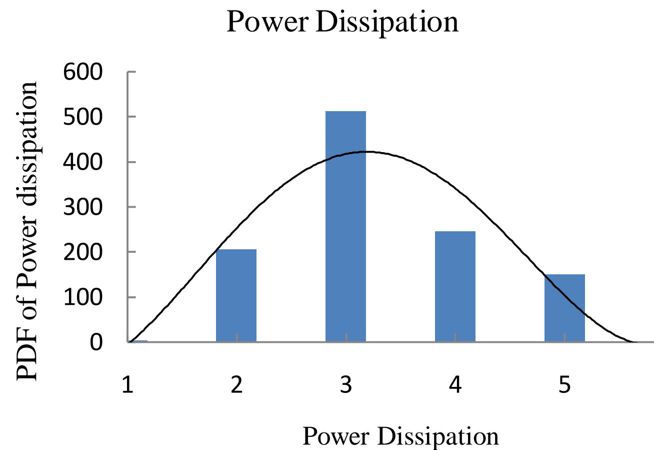

Fig. 10. Probability distribution function for power dissipation obtained using Monte-Carlo simulation.

Monte-Carlo is a simulation technique that depends on repeated random sampling and thereafter performing

analysis to compute the results. In Monte Carlo simulation, first of all, input parameters under consideration are sampled within the deviation range. For each sample of input parameters, there will be set of output parameters. The value of each output parameter is outcome of each simulation run. Subsequently, the output is collected and computed that is obtained from each simulation runs. Thereafter statistical analyses on these obtained values are performed. Probability distribution function (PDF) is the method to map each random signal [20]. In the present Monte-Carlo analysis, all the parameters under consideration are varied simultaneously by $\pm 3\sigma$ [28]. In this analysis, power dissipation and delay are calculated by varying all the parameters together. Monte Carlo analysis is used in order to understand the effect of process variation on MLGNR interconnects. This analysis requires a large number of simulation trials. Analysis is performed at 25°C and 1000 runs have been considered. PDF is obtained for propagation delay and power dissipation by varying all input parameters by $\pm 3\sigma$. The PDF for delay and power dissipation are shown in Figs. 9 and 10 respectively. From Figs. 9 and 10, it is seen that the mean values of PDF in case of delay and power dissipation are 8ns and 0.3nw respectively. The standard deviation values for former and latter are 4ns and 0.6nw respectively. The lower value of graphene in subthreshold region shows that variability effect is lower in graphene as compared to copper.

Conclusion:

The present paper details about the variability analyses of graphene interconnect in subthreshold region of operations. It is analyzed that MLGNR is better interconnect material in terms of lower power dissipation and delay in subthreshold region as compared to copper interconnect. Variability analysis gives the performance of overall system with respect to parameter deviations. The different variability analyses have been performed. It is analyzed that FF process corner model results in lesser delay while SS process corner model leads to lesser power dissipation in the circuit. In parametric analysis, effects of variation in different parameters have been analyzed. It is seen that for all the variation of parameters, graphene interconnect outperforms copper interconnect. From the Monte-carlo analysis, it is also seen that graphene has lesser standard deviation than copper interconnect. Henceforth conveying its higher performance than copper interconnect. Hence from the present work, it can be convincingly deduce that graphene interconnect is aptly suitable for next generation high performance interconnect with lower impact of variability effects.

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