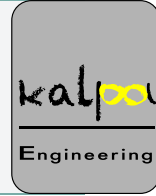




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## DSTATCOM for Harmonics Mitigation in 3-Phase 3-Wire System

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### Abstract

Distribution systems have been facing serious problems of harmonics load current mainly due to advancement in power electronic based and other non-linear loads. The DSTATCOM has been widely used to mitigate the load current harmonics problems in distribution system. In this paper design and simulation of DSTATCOM with SRF Control Strategy is carried out with 3-phase 3-wire distribution system to mitigate the harmonics load current problem using MATLAB /SIMULINK software.

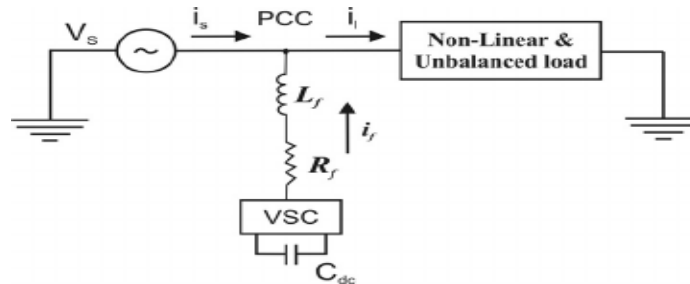
**Keywords—**harmonic; DSTATCOM; SRF; Distribution System

## 1 Introduction

Distribution system now days are facing several power quality problems like poor power factor, poor voltage regulation, harmonics current burden, unbalanced loading, neutral current excess etc.[1, 2] Harmonics current is mainly because of use of non-linear nature of load and poor power factor and poor voltage regulation is mainly due to the inductive load and line drop respectively. IEEE-519 standard is proposed to control harmonics current.

The Followings are the effect of harmonics on the various equipments:

1. Damage to the capacitor bank
2. Transformer derating
3. Induction machine crawling
4. Increase of Hysterisis and eddy current losses
5. Interference with communication system
6. Protective devices malfunctioning



**Figure 1:** Single Line Diagram of DSTATCOM

Many Custom Power Devices like DVR, UPQC are proposed for mitigating the power quality problems in distribution system.[3] Distribution Static Compensator is shunt connected device which is able to mitigate load current based power quality problems. It injects compensating current such that load current based power quality problems like voltage sag, voltage swell, unbalance loading, poor power factor, poor voltage regulation, harmonics etc. can be mitigated using the DSTATCOM[4, 5].

Many topologies for 3-phase 3-wire and 3-phase 4-wire distribution static compensator has reported in the literature. Some of the 3-phase 3-wire DSTATCOM configurations are three single VSC based, two leg VSC with split capacitor based, 3-leg VSC based DSTATCOM. For control of DSTATCOM many control strategies like SRF theory, p-q theory, Unit template and Hysterisis control, Power balanced theory have proposed in the literature[5-7].

In this paper 3-leg VSC based DSTATCOM with SRF Control Strategy is used to mitigate the harmonics problem due to non-linear load. Figure 1 shows the single line diagram of the DSTATCOM.

## 2 Basic Theory

Figure 2 shows the generalized diagram of DSTATCOM for 3-phase 3-wire distribution line with the control strategy. DSTATCOM is connected in shunt with the load at the PCC. The DSTATCOM is comprised of 3-leg Voltage Source Inverter with capacitor at the DC link and connected to the distribution line through the interfacing inductor. Capacitor here acts as the energy storage element and inductor is used to reduce the ripple in the current. DSTATCOM can either be used for power quality improvement or for the power flow control in the line. If one wants to use the DSTATCOM for Active Power Flow in the line in that case the energy storage element required is either Battery Energy Storage or the Voltage Source[1].

Load current is sensed and applied to the control strategy and reference source current are generated. Control signal can be generated either by the PWM or by the Hysteresis current control. In the PWM control reference source current is compared with the triangular wave and according to intersection between the two signal the gating pulses are generated. In the Hysteresis current control, the reference source current is compared with the actual source current and according to the Hysteresis band gating signal are generated. DSTATCOM will inject the harmonic current such that it will nullify the effect of load current harmonics on the source side.

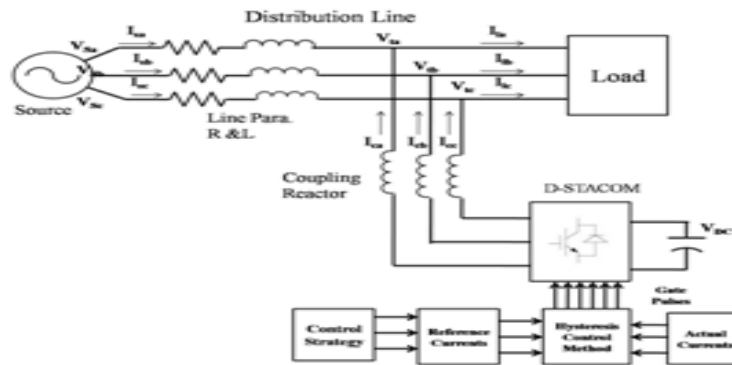


Figure 2: Generalized diagram of DSTATCOM

## 2.1 Design of parameter

IGBT with anti-parallel connected diode is used to the construct the VSC. IGBT is used to construct the VSC because the IGBT is low power device, switching frequency is also medium, there is no problem of second breakdown like BJT, and is comprised theadvantages of both MOSFET and BJT. The anti-parallel connected diode is used to provide the pathfor charging of DC linkcapacitor. The rating of switch can be selected using the following equation (1).

$$V_{sw} = V_{DC} + V_d \tag{1}$$

$V_{sw}$  = Switch Voltage rating  
 $V_{dc}$  = DC Bus Voltage  
 $V_d$  = 10% overshoot in DC bus Voltage

The current ratings of the IGBT switch can be calculated using the equation given below.

$$I_w = 1.25(I_{cr} + I_{sp}) \tag{2}$$

$I_{sw}$  = Switch Current rating  
 $I_{cr}$  = ripple current  
 $I_{sp}$  = peak current Capacitor

Switch voltage and current rating should be higher than the calculated value so for safety purpose in case of any abnormal condition occurs in the system.

DC bus voltage of the capacitor must be greater than the twice of the phase voltage of the system otherwise the DSTATCOM cannot supply the compensating current to the system. In case of Active Power Flow control using DSTATCOM one need to use either battery energy storage or a voltage source but for only reactive power flow control capacitor alone can be used as energy storage. DC bus voltage can be calculated using the equation (3).

Where

$V_{dc}$  = DC Bus Voltage,  $V_{LL}$  = Line to Line Voltage of the system,  $m$  = modulation index

$$V_{DC} = 2\sqrt{\frac{2}{3}} \frac{V_{LL}}{m} \quad (3)$$

The value of the capacitor depends upon the energy balanced Equation and can be calculated using equation (4).

$$\frac{1}{2} C_{DC} (V_{DCref}^2 - V_{DC}^2) = 3V_{ph} aIt \quad (4)$$

$C_{dc}$  = DC Bus capacitor,  $V_{DCref}$  = reference DC bus voltage,  $V_{DC}$  = minimum value allowed of reference DC bus voltage,  $V_{ph}$  = phase voltage,  $a$  = overloading factor which is taken generally as 1.2,  $I$  = current at output of the DSTATCOM,  $t$  = time by which energy should be recovered during transient.

The interfacing inductor is used to smoothing out the compensating current. The ripple is reduced by using the interfacing inductor. The ripple in the current are introduced due to the firing of different switches. If the switching frequency is higher in that case the ripple is much less but switching losses increases to great extent.

The interfacing inductor value is directly proportional to dc bus voltage and inversely proportional to the ripple current and switching frequency as given in equation (5).

$$L_f = \frac{\sqrt{3}mV_{DC}}{12af_s I_{Crpp}} \quad (5)$$

$L_f$  = interfacing inductor,  $m$  = modulation index and is generally taken as 1 for the most of the DSTATCOM configuration,  $V_{dc}$  = DC Bus Voltage,  $a$  = overloading factor which is taken generally as 1.2,  $I_{crpp}$  = ripple current.

### 3 Control Strategy

Many control schemes have been introduced in the literature like SRF, p-q theory, power balanced theory, unit template and Hysterisis current control and most widely used control scheme is Synchronous reference frame theory based. Synchronous Reference Frame theory is also called as SRF, d-q-o theory or Parks transformation. DC bus voltage, load current, and source voltage and source current are sensed and used in this control scheme. 3-phase load current  $I_a$ ,  $I_b$ ,  $I_c$  are sensed and converted into d-q-0 form as given in below equation.

$$\begin{pmatrix} I_{Ld} \\ I_{Lq} \\ I_{L0} \end{pmatrix} = \frac{2}{3} \begin{pmatrix} \cos(\theta) & \cos\left(\theta - 2\frac{\pi}{3}\right) & \cos\left(\theta + 2\frac{\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - 2\frac{\pi}{3}\right) & \sin\left(\theta + 2\frac{\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix} \begin{pmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{pmatrix} \quad (6)$$

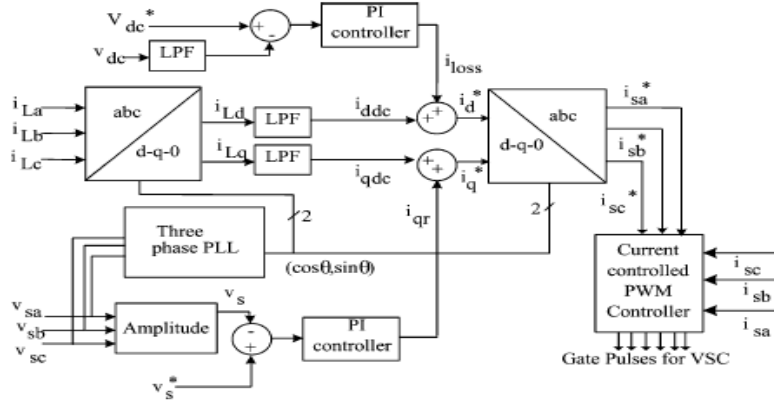


Figure 3: SRF Control Scheme

Reference source current can be obtained using the inverse d-q-0 transformation

$$\begin{pmatrix} I_{sa}^* \\ I_{sb}^* \\ I_{sc}^* \end{pmatrix} = \begin{pmatrix} \cos \theta & \sin \theta & 1 \\ \cos\left(\theta - 2\frac{\pi}{3}\right) & \sin\left(\theta - 2\frac{\pi}{3}\right) & 1 \\ \cos\left(\theta + 2\frac{\pi}{3}\right) & \sin\left(\theta + 2\frac{\pi}{3}\right) & 1 \end{pmatrix} \begin{pmatrix} I_{Ld}^* \\ I_{Lq}^* \\ I_0^* \end{pmatrix} \quad (7)$$

$I_{Ld}$  and  $I_{Lq}$  both contains dc and ac components due to the harmonics present in the system and ac component components are removed using the either low pass filter or the mean block in case of the simulation.

$$I_{Ld} = I_{ddc} + I_{dac} \quad (8)$$

$$I_{Lq} = I_{qdc} + I_{qac} \quad (9)$$

Reference direct axis current is obtained by the adding the  $I_{ddc}$  and  $I_{loss}$  where  $I_{dloss}$  component is output of PI controller.

$$I_d^* = I_{ddc} + I_{dloss}$$

$I_{Lq}$  depends upon for which operation DSTATCOM is operating either UPF (Unity Power Factor) or ZVR (Zero Voltage Regulation). For UPF operation the reactive power supplied by the source is zero and all the reactive is supplied by the DSTATCOM.

$$I_q^* = 0 \text{ (for unity power factor operation)} \quad (10)$$

For ZVR mode of operation both source and DSTATCOM must supply the reactive power to the load and to maintain the PCC voltage at the nominal value thus keeping voltage regulation zero.

$$I_q^* = I_{qdc} + I_{qloss} \text{ for ZVR operation} \quad (11)$$

3-phase PLL (Phase Lock Loop) system is used for synchronizing purpose. Obtained Reference source current are compared with triangular wave in case of PWM control signal generation technique and according to the I the intersection between the reference source current and the

triangular wave the control signals are generated. In case of Hysteresis current control technique the reference source currents are compared with the actual source current and according to the Hysteresis band the control signals are generated.

### 4 Simulation and Results

Simulation is carried out with the following system data using the matlab/Simulink toolbox. Simulation circuit is shown in Figure 4. source is 3-phase, 415 volt, 50 Hz is delivering power to the non-linear load which is 3-phase bridge with diode rectifier and resistance of 60 ohm at the DC bus through the 3-phase 3-wire distribution system. Load is non-linear so draws discontinuous current from the source but DSTATCOM injects compensating current such that the source

current remains sinusoidal Fig 5 shows the 3-phase source voltage, load current of the phase a  $I_{La}$ , compensating current of the phase a  $I_{Ca}$ , source current of Phase a  $I_{Sa}$  respectively.

Sr.No.	parameter	Value
1	source	415 volt,50 HZ
2	load	Universal bridge with R=60 ohm
3	DC bus voltage	700 volt
4	Capacitor	3000 $\mu$ F
5	Interfacing Inductor	2.5 mH
6	$K_{pd}, K_{id}$	4.8 ,72.2
7	$K_{pk}, K_{iq}$	0.0008, 0.006

Table 1: simulation parameter

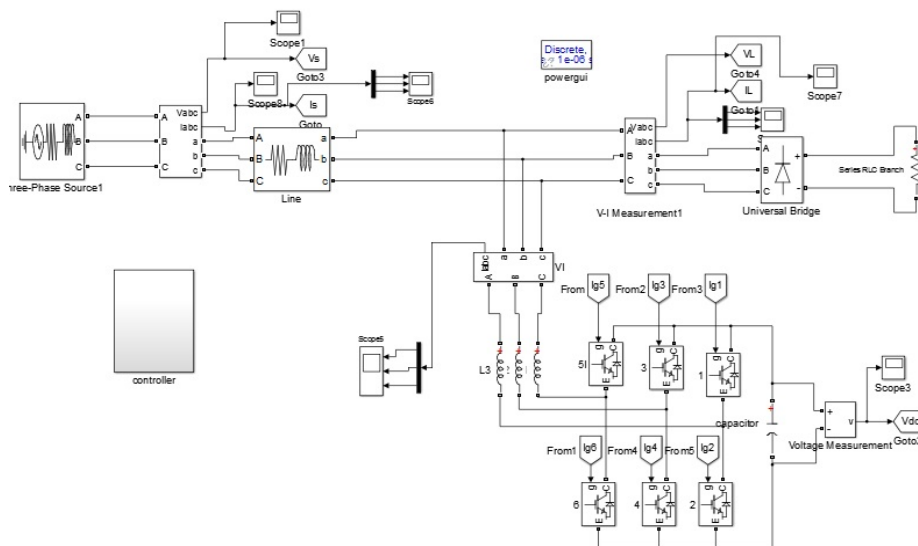


Figure 4: Simulation Diagram

Source voltage is ideal sinusoidal with 415 volt rms and is balanced condition as shown in Figure 5. Figure 6 shows the load current is nonsinusoidal due non linear behaviour of load which is reflected back on source side so source current is also non sinusoidal without compensation. DSTATCOM injects the compensating harmonic current such that the source current remains sinusoidal even though the load current is non sinusoidal.

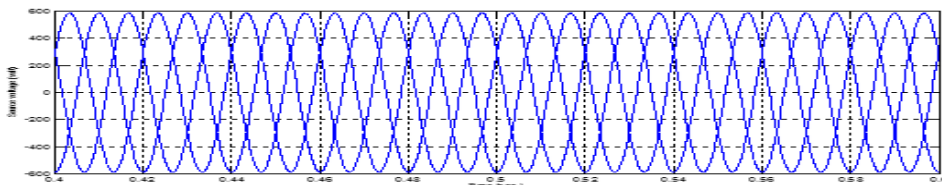


Figure 5: Source Voltage

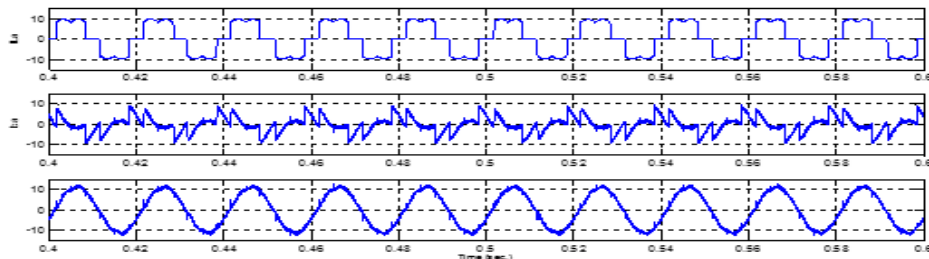


Figure 6: load, compensating and source current

Capacitor is used as energy storage element the DC voltage of it needs to be regulated at the constant value of reference. For that purposed we used the PI controller which maintained the dc bus voltage constant at 700 Volt

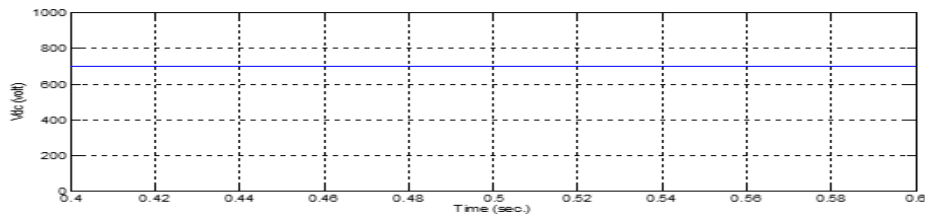


Figure 7 Dc bus voltage

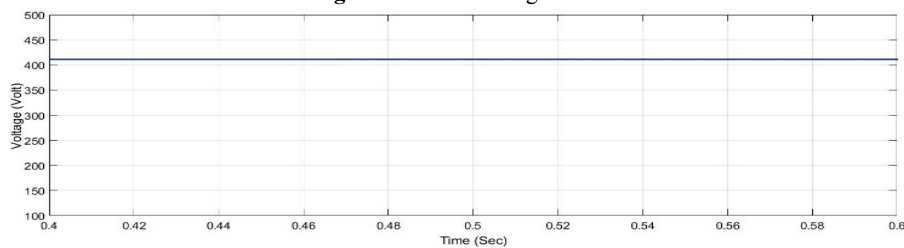


Figure 8: PCC Voltage

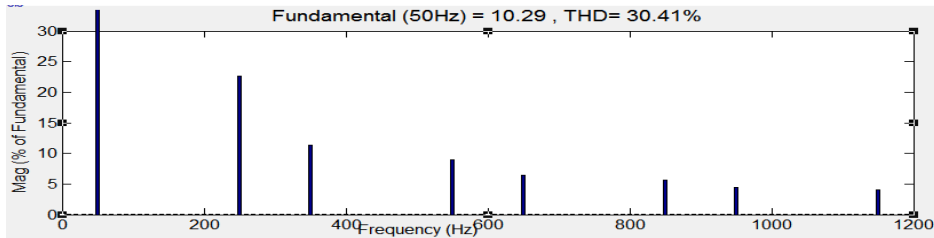


Figure 9: Load current THD

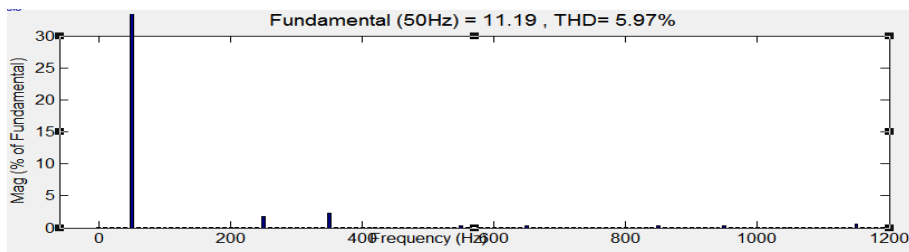


Figure 10: Source current THD

To make the voltage regulation zero another PI controller is used which maintains the load voltage at nominal value by making regulation zero. Figure 7 shows the DC bus voltage whereas the Figure 8 shows the RMS value of the load voltage which indicates the zero regulation. The factor THD is Total Harmonic Distortion and can be evaluated by ratio of Root Mean Square of Harmonic current to Root Mean Square of fundamental current expressed as percentage of fundamental. Figure 9 shows the load current THD which is 30.41% and Figure 10 shows the source current THD which is 5.97%.

## Conclusion

Due to use of non-linear load the harmonics are introduced which is the main severe problem in distribution system. Simulation results shows that the DSTATCOM using the Synchronous Reference Frame theory is able to maintain the PCC voltage at Reference value by using the PI controller and also maintains the DC bus voltage at the reference value using the PI controller. Simulation results shows that it reduces the THD from 30.41% to 5.97%.

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